INTERIM RESEARCH REPORT NO. 11A

PROJECT

lightning

HIGH-SPEED DATA PROCESSOR SYSTEM RESEARCH

Prepared for **DEPARTMENT OF THE NAVY**
Bureau of Ships, Washington 25, D.C.

Prepared by **RADIO CORPORATION OF AMERICA**
Camden, New Jersey

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for

HIGH-SPEED DATA PROCESSOR SYSTEM RESEARCH

Project LIGHTNING

This report covers the period of June 1, 1961 to August 31, 1961

Prepared for

DEPARTMENT OF THE NAVY

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Prepared by

Engineering Department
Electronic Data Processing Division
Industrial Electronic Products

RADIO CORPORATION OF AMERICA

Camden, New Jersey

TABLE OF CONTENTS

Chapter 1. GENERAL

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1-1 INTRODUCTION

This quarter's work concentrated upon completing the frozen designs, both electrical and mechanical, and beginning construction of the subsystem. To be completed during Phase III B, this subsystem will demonstrate feasibility of the techniques developed during the course of Project LIGHTNING.

The worst-case designs of the logic subsystem were finalized during the quarter, and all types of wafers were constructed and tested. Performance of these wafers was essentially in agreement with analytic calculations. It is now believed that the subsystem can be built with no further key invention required.

Specifically:

1. Diodes

(a) All types of tunneling devices required have been built within specification. At present, however, delivery of the OR - type tunnel rectifier is a key problem.

(b) There has been no observed deterioration of the GaAs units as designed to operate the subsystem. We therefore believe that this is no longer a problem.

(c) A change from diffusion-to solution-grown GaAs crystal has been affected which will allow us somewhat greater latitude in tolerance design of memory drivers.

(d) The problem of tunneling device solderability has been corrected with device fabrication change.

2. Logic Circuits

(a) The worst-case design of these circuits is essentially complete. Any changes in design hereafter will be made in order to improve the delivery schedule of tunneling devices.

(b) The AND gate design described in the last report was changed as a result of our inability to supply sufficient tunneling devices. The present AND gate is a modification of a thresholding-type circuit described sometime ago.

(c) The OR and the bistable gates proposed for the subsystem are essentially those described in the last report.

(d) A special delay wafer was designed, built and released to the subsystem group.

3. Fabrication

(a) The present wafer has been finalized and designed with dimensions of 1-1/2 inch by 6/10 inch to 7/10 inch. The variation in width is dependent upon the type circuit enclosed.

(b) Frame construction is open type to allow free access of cooling air.

(c) Wafer-to-wafer interconnection will be made by specially developed drawn-copper coaxial lines. These will be soldered in place to the wafers.

(d) The d-c low-impedance distribution lines are mounted in the side frames for direct connection to the wafers being supplied.

4. Subsystem

(a) All the parts for the subsystem have been ordered and delivery is underway.

(b) A problem of resistor supply has developed and we are working with back-up vendors. We have now developed five potential suppliers.

(c) At the present time we are making use of trimming techniques to assist in supplying resistors within the tolerance limits.

(d) Several wafers have been operated together in design fashion. Repetition rates are equal to or better than those originally expected.

(e) D-c distribution lines are being fabricated within the house and these appear to have answered the requirement adequately.

(f) The frame layout for the logic subsystem is nearing completion and most parts required have been ordered.

5. Memory Circuits

(a) Two of the three planes of the nine-word system have been operated for periods of time up to a complete weekend. The third plane is ready to be installed.

(b) This system is being operated at a repetition rate of 43 megacycles corresponding to regeneration time of 23 nanoseconds. This is actually faster than our goal time of 25 nanoseconds.

(c) The milling of all frames for the 32-word system is complete and drive lines are mounted in place.

(d) The worst-case analysis of all circuits is well underway, and most of the components are ordered.

1-2 INTERPRETIVE SUMMARY

The emphasis during Phase IIIB applies first priority to the construction of a feasibility model to be demonstrated during the phase.

A. GENERAL

The work on the design and construction of the logic subsystem was rescheduled during the early part of the quarter (July). All areas of the schedule have been bracketed with the exception of tunneling devices and resistor delivery.

A generalized program was written which will now allow us to test on a digital computer the operation of most types of tunnel diode digital circuits.

All the chosen circuits have been operated and the laboratory performance shows good agreement with the analytical calculations.

B. DEVICES AND C)MPONENTS

We have developed multiple suppliers for resistors and we now have five vendors capable of meeting our specifications.

In addition to this approach, we have developed our own capability in the so-called trimming process, in which we modify the resistor value by mechanical means. This method has proved useful in constructing wafers where resistors of critical values were unavailable.

Considerable difficulty has been encountered in supplying the required quantities of tunneling devices within specification. This can mean that our manufacturing schedule may be delayed as much as two months, a time which will subtract from our presently scheduled four month test time.

Our chosen circuits were frozen to tunnel device specifications which we had seen in sample delivery. We subsequently met unexpected difficulty in fabricating to these specifications and began to wonder if such were wise. It is our opinion that the best course of action is to stay within these specs.

A special console for precision measurement of tunnel diode parameters is being constructed. This console will be capable of measuring all current and voltage parameters to an accuracy of one-tenth percent. There will be primary and secondary standards measurement facilities, both capable of the aforementioned accuracy. This console will be operational during September.

The problem of tunnel diode parameter change with soldering has been surmounted and is no longer considered a serious situation.

C. LOGIC CIRCUITS

The circuits for the subsystem were finalized with worst-case design information completed. Essentially, these are the same circuits described in the last report with the exception of the AND wafer. Because of inability at this time to obtain special diodes required for our previously specified AND gate, we have shifted over to a threshold gate which, although somewhat more complicated and slightly slower, can be built with presently available tunneling devices. The worst-case designs completed for all circuits were done by both analog and digital computation.

A special delay circuit was designed, laid out on a wafer and released to the subsystem group for incorporation into the logic subsystem.

Precise measurement techniques were developed for examining tunnel diode properties including internal inductance and capacity. Further component measurements were performed on the characteristic impedance of the special miniature coax, including reflected waveforms. A considerable effort concentrated on the measurement of resistor properties, under derated load, normal load and operation in excess of normal load. Most of the changes noted were traceable to mechanical change in the end connections and damage resulting from improper handling. Consequently, a special tool was designed which could solder both ends of the resistor simultaneously.

Further crosstalk measurements were performed in an effort to forecast the magnitude of this problem in the subsystem.

All major fabrication decisions for the subsystem have now been made. The present wafer length has been increased to 1-1/2 inches with a width of 6/10 to 7/10 of an inch depending upon the type of wafer. There are three basic types of wafer performing an AND, an OR and a bistable store logic function. An additional wafer to perform a delay function was also designed. The present open frame design will allow free-air circulation around the wafers, and wafer interconnection is to be done by means of coaxial cables which are connected point-to-point and soldered in place.

Operation has been accomplished of all wafers performing singly in accordance with the computed analysis. Several of these wafers have been operated together in a frame utilizing the d-c distribution techniques of low-impedance transmission lines. Again, operation in this manner appears to be in accordance with that predicted.

All the parts for this subsystem have been ordered and many received. One of the key problems here was considered to be that of fabricating the wafer holders. We had planned to have these pieces built by an outside vendor, but because the internal cost per unit reduced considerably over our first estimate, we have been building them within the house. Most have been received. We are currently working in close cooperation with several vendors on the problem of supplying precision resistors. At the present time, this does not appear to be an insuperable problem; it is being solved by working with more vendors.

Our systems layout design is nearing completion, as is the frame layout for the logic subsystem. Most parts for the frames have also been ordered.

D. MEMORY

Our memory activity is essentially on schedule and two of the three planes for the nine-word system are operational with the third ready to be installed. This nine-word system is actually regenerated in a 12 nanosecond cycle time; but because of recovery time of the drivers, it operates at a repetition rate of 43 megacycles which corresponds to about 23 nanoseconds.

Our goal cycle time for the 32-word subsystem is actually 25 nanoseconds.

We have operated this system for relatively long periods of time with good results. The system has been run over night and through weekends with several locations continuously regenerated.

To date, there has been no deterioration observed of the GaAs tunnel diodes in the nine-word system.

The milling is complete on all of the frames for the 32-word system, and the word and digit lines are mounted in place. The tunneling device holders are completely installed on one plane and installation is underway on the others.

Our worst-case analysis is well along, and as a result, all the components are ordered—many were received.

A change to solution-grown GaAs tunnel diode driver construction has been affected during the quarter. This change gives wider latitude to the design of the word and digit drive circuits.

1-3 OBJECTIVES AND SCHEDULES

Most of the mechanical construction will be done during the second quarter, and electrical testing of the wafers and subsystem frames will begin.

1. Devices

(a) All effort will be focused on obtaining solution to the problem of supplying tunneling devices in quantities great enough to complete construction of the subsystem.

(b) Instrumentation presently under construction will be put into operation for reading electrical parameters of the tunneling devices.

(c) A new package of extremely low capacity will be evaluated for possible use with tunnel rectifiers.

(d) All the GaAs tunneling devices will be fabricated using the solution-grown method.

2. Logic Circuits and Fabrication Studies

(a) Back-up design analysis for the subsystem will continue.

(b) Design improvement analysis will continue.

(c) Statistical study on reliability of the resistors will be continued.

(d) Both theoretical and practical analysis of the associated heat problems will be carried out.

3. Logic Subsystem

(a) Most of the wafers required for the subsystem will be built and tested.

(b) All of the component parts of the subsystem will be received.

(c) Power supplies will be ordered.

(d) Test sets for components, wafers and frames will be put into operation.

(e) A test position to facilitate resistor "trimming" will be put into operation, as a back-up for the resistor delivery.

4. Memory

(a) All subsystem components will be received.

(b) The power supplies will be delivered.

(c) The sense amplifier and memory drivers required to drive the first 32-word plane will be fabricated.

(d) The first plane will be tested.

(e) All memory planes will be fabricated.

(f) Decoder construction will begin.

Chapter 2. LOGIC CIRCUIT DEVELOPMENT

SUMMARY

Major effort in the area of logic circuits during the quarter has been in establishing and optimizing a set of circuits for the subsystem. More specifically:

- A set of logic circuits has been chosen, and nominal values of all components as well as allowable tolerances were specified.
- Both analog and digital computer facilities have been used extensively in circuit optimizing and some worst-case conditions of operation have been checked with the computer.
- A worst-case tolerance analysis has been used in conjunction with dynamic computer simulation and laboratory results to arrive at circuit designs.
- All chosen circuits have been operated on wafers in the laboratory and results to date have agreed favorably with computed results.
- A delay circuit has been designed to provide delays required in the subsystem.
- Work is in progress on a generalized program which will be useful for analyzing most typical circuit configurations.
- Initial results have been obtained from a digital computer simulation of transmission line circuit interconnections.

Chapter 2. LOGIC CIRCUIT DEVELOPMENT

I. PERSONNEL

The following personnel contributed to this phase of the product during the eleventh quarter:

L. Almeleh
R. H. Bergman
R. Chueh
M. Cooperman
E. C. Cornish
D. M. Durr
H. R. Kaupp
M. McLean
J. F. Page
C. Pendred
H. Ur

II. DISCUSSION

A. DESIGN OF MONOSTABLE "OR" GATES AND "AND" GATES

1. General

The data which follows describes the design of monostable-threshold OR and AND gates for the logic subsystem. The threshold type AND gate was chosen for use in the subsystem upon discovery of the problems associated with the diode-type AND gate.

Choice of the threshold-type AND gate necessitates close control of the output voltage from driving stages. This requirement is felt to be ultimately undesirable, but it represents the best utilization of currently available tunnel diodes and tunnel rectifiers.

Paragraphs 2. through 7. which follow delineate the tunnel diode, tunnel rectifier, power supply, transmission line, and logic gate specifications utilized for the design of the monostable OR and AND gates.

2. Specifications for Tunnel Rectifiers

(a) Clamping Diode

$V_{c\ 60}$ = 205 mv ±7%

I_p = 0.7 ma max.

C = 8 pf max.

(b) OR Diode

V_c 7.5 = 162 mv ± 5%

I_p = 0.2 ma max.

C = 1 pf max.

I at -500 mv = 1 ma max.

(c) AND Diode

V_c 10 = 114 mv ± 5%

I_p = 0.5 ma max.

C = 3 pf max.

3. Specifications for Germanium Tunnel Diodes

(a) 25-ma unit

I_p = 25 ma ± 1%

E_p = 96 mv ± 5%

E_v = 390 mv ± 5%

E_f = 555 mv ± 5%

I_p/I_v = 10 min.

C = 6 pf max.

(b) 50-ma unit

I_p = 50 ma ± 1%

E_p = 99 mv ± 5%

E_v = 400 mv ± 5%

E_f = 550 mv ± 2%

I_p/I_v = 10 min.

C = 12 pf max.

(c) 20-ma unit

I_p = 20 ma ± 1%

E_p = 96 mv ± 5%

E_v = 390 mv ± 5%

E_f = 555 mv ± 5%

I_p/I_v = 10 min.

C = 4.8 pf max.

(d) 35-ma unit

I_p = 35 ma ± 1%

E_p = 96 mv ± 5%

E_v = 390 mv ± 5%

E_f = 550 mv ± 2%

I_p/I_v = 10 min.

C = 7.9 pf max.

4. Specifications for Power Supplies

(a) +6 volts ± 2%

(b) +100 mv ± 10%

(c) Resistance of power supplies - nominal value ±1%

5. Specifications for Signal Transmission

(a) Characteristic impedance of coaxial cable = 25.7 ohms ± 2%

(b) Trimmed OR tunnel rectifier at sending end or receiving end of OR gate.

I at 170 mv = 7.5 ma + 4%

(c) Resistance termination at receiving end of AND gate:

21.8 ohms ± 1% for level input from bistable circuit.
22.7 ohms ± 1% for pulse input from another monostable circuit.

6. OR Gate

(a) The OR gate receives pulse inputs. When one or more inputs are high, a reshaped pulse appears at the output terminals. Figure 2-1 is a complete circuit diagram of the OR gate with cascaded, tunnel-diode monostable circuits for pulse amplification.

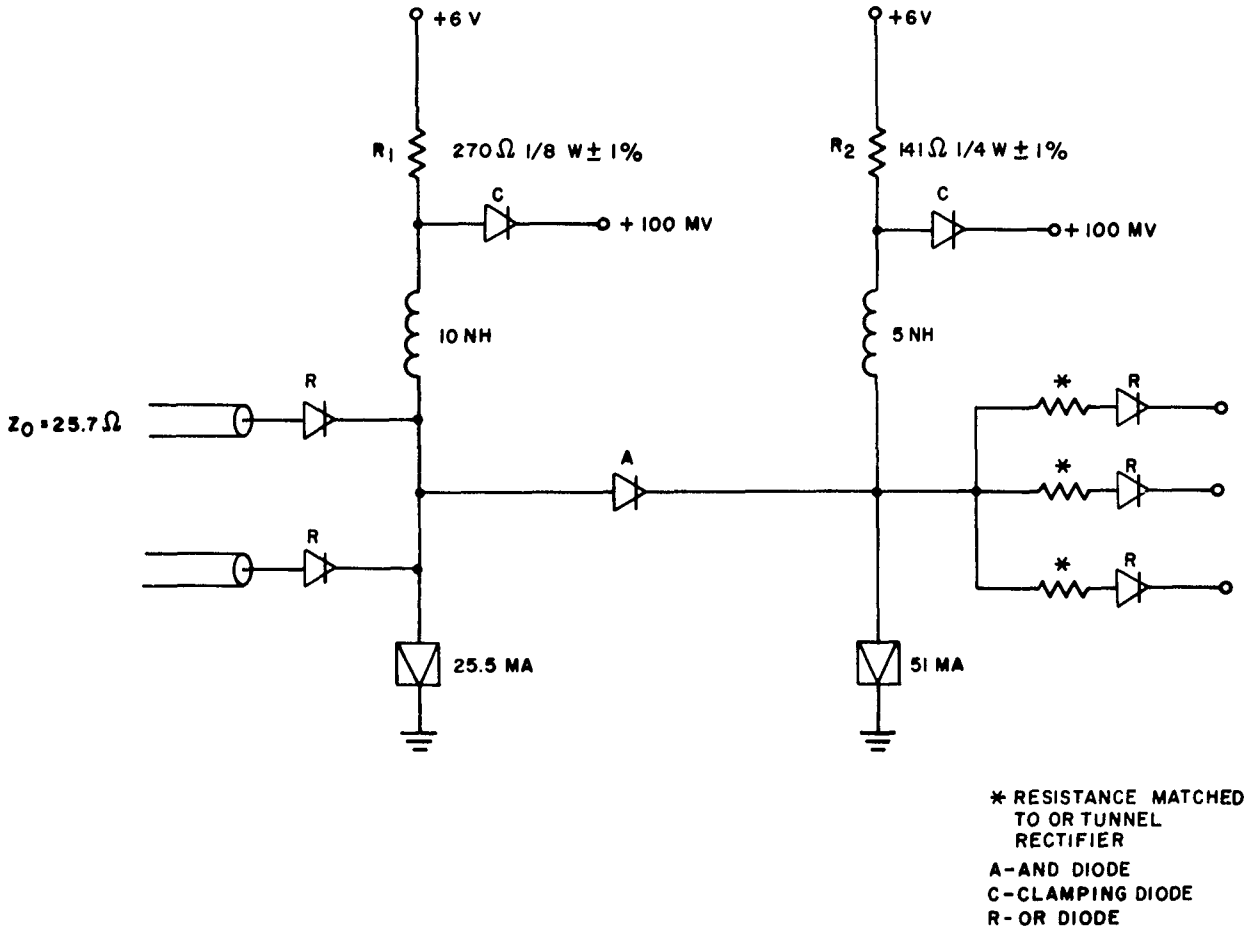


Figure 2-1. OR Gate Circuit

(b) Input Specifications

The output pulse from the 50-ma tunnel-diode monostable circuit must be as follows:

(1) Amplitude $\geq$ 450 mv

(2) Width (when amplitude is equal to or larger than 450 mv) $\geq$ 0.5 ns.

(3) Current loading of each input at 450 mv = 7.7 ma minimum; 9.3 ma maximum

The maximum fan-in is 5, but a fan-in of only 2 is assumed in all the following calculations:

(c) Output Specifications

To meet the input specifications of the AND gate, the OR gate and the inverter, the maximum fan-out of this OR gate is 3.

(d) Signal propagation speed and maximum repetition rate of this gate is primarily determined by the circuit configuration in the actual layout.

7. AND Gate

(a) The two-input AND gate has one level input from a bistable circuit and one pulse input from an OR gate or another AND gate. Only when both inputs are high does a reshaped pulse appear at the output terminals. Figure 2-2 is a complete circuit diagram of the AND gate. A threshold AND logic function is performed by TD_1, while TD_2 and TD_3 are cascaded monostable circuits for pulse amplification.

(b) Input Specifications

(1) Level Input

Voltage: From 450 mv to 510 mv

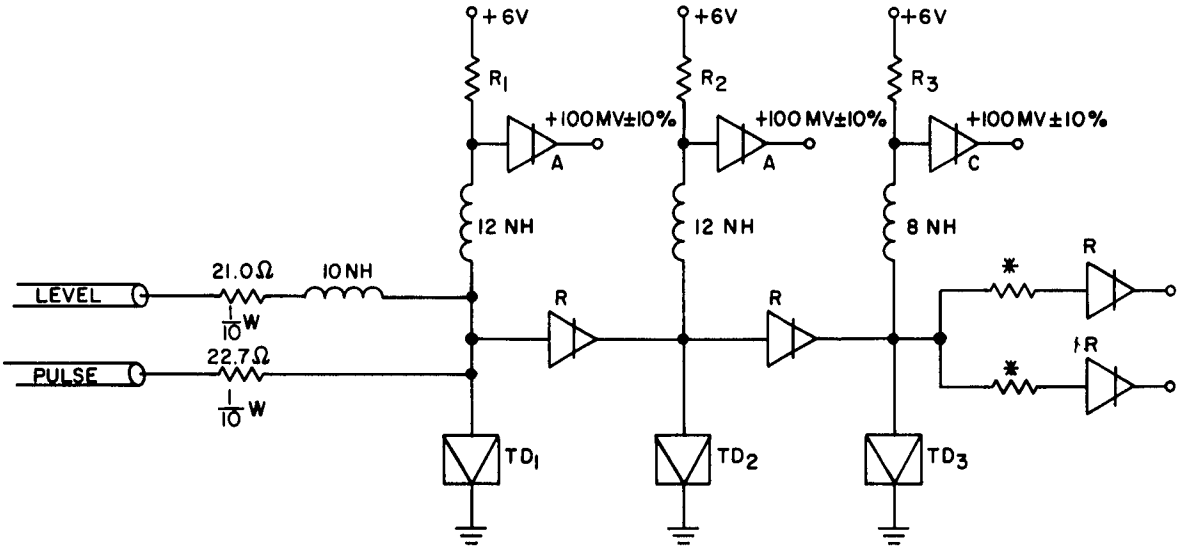
Current: From 8.1 ma to 10.1 ma at 450 mv

(2) Pulse Input

Voltage: From 450 mv to 530 mv

Current: From 7.7 ma to 9.6 ma at 450 mv

Pulse Width: Larger than 0.5 ns



TD_1	19.6 MA	20.0 MA	
R_1	1100 Ω	1027 Ω	1/10 W

TD_2	20.0 MA	20.4 MA	
R_2	340 Ω	333 Ω	1/8 W

TD_3	34.3 MA	35 MA	35.7 MA	
R_3	202 Ω	206 Ω	211 Ω	1/4 W

Figure 2-2. AND Gate Circuit

(c) Output Specifications

To meet the input specifications of the AND gate, the OR gate and the inverter, the maximum fan-out of this AND gate is 2.

(d) Signal propagation speed and maximum repetition rate of this gate is primarily determined by the circuit configuration in the actual layout.

8. Design Assumptions:

The above specifications and circuit component values were calculated on the basis of the following assumptions. These assumptions seem realistic in the light of present knowledge.

(a) Tolerance of ±1% resistors is calculated at ±2%, considering temperature and aging effects.

(b) A ±2% is used as the tolerance of tunnel-diode peak current which is ±1% initially.

(c) A minimum I_p/I_v ratio of 9 is used in calculations instead of 10 because of the temperature effect on the minority carrier region.

(d) Figure 2-3 shows the total variation of the 50-ma tunnel-diode V-I curve in the high voltage region. The two right-hand curves show initial tolerance among components and th left-hand curve shows the extreme effects of the combination of a heavy duty cycle and a 12 degree rise in room temperature (a temperature coefficient of 1.1mv/°C).

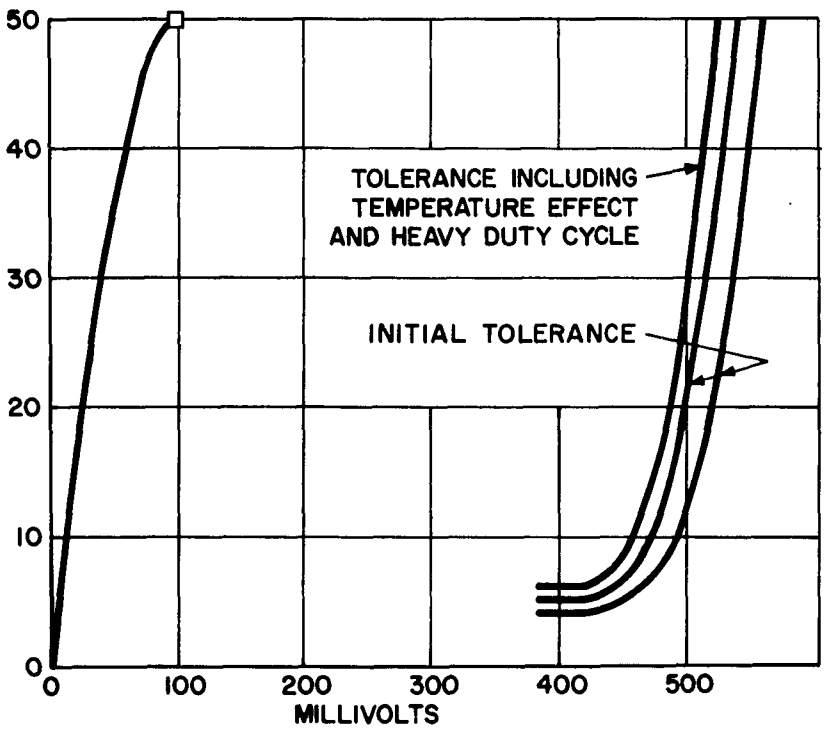


Figure 2-3. Variation of Tunnel Diode V-I Curve at High-Voltage Region

(e) The output voltage variation of the bistable circuit is assumed to be between 450 mv and 510 mv. This is derived as a result of:

(1) Total variation of the output tunnel diode's V-I curve as shown in the two extreme curves of Figure 2-3.

(2) The variation of loading currents.

(3) The variation of the transient trajectory of the output stage.

(4) The unbalance of inductance among loads.

(f) The output voltage variation of a monostable circuit is assumed to be between 450 mv and 530 mv. This is derived as a result of:

(1) Total variation of the output tunnel diode's V-I curve.

(2) The variation of loading currents.

(3) The variation of the transient trajectory of the output stage.

(4) The unbalance of inductance among loads.

(5) The tolerance of the clamping circuit inductance.

(6) The variation in the lengths of the connecting signal lines and the variations in the delays in the receiving circuits being triggered.

(g) Coaxial transmission lines of the same characteristic impedance are used for all signal connections between stages.

(h) In the calculation of the AND gate input current, a + 10% tolerance is allowed for signal transmission. It is assumed that after the risetime is over, the relation of

$$i = \frac{V}{2Z_o} (1 + 10\%)$$

will be satisfied (Figure 2-4). The assumed + 10% tolerance consists of resistor tolerance, trimmed tunnel rectifier tolerance and reflection due to mismatched transmission lines.

(i) In the design of each monostable circuit, a 5% of I_p is assumed as safety bias and a 7% of I_p as overdrive for triggering. At the monostable circuit of the output stage, a 4% of I_p is estimated as the current shared by the clamping circuit.

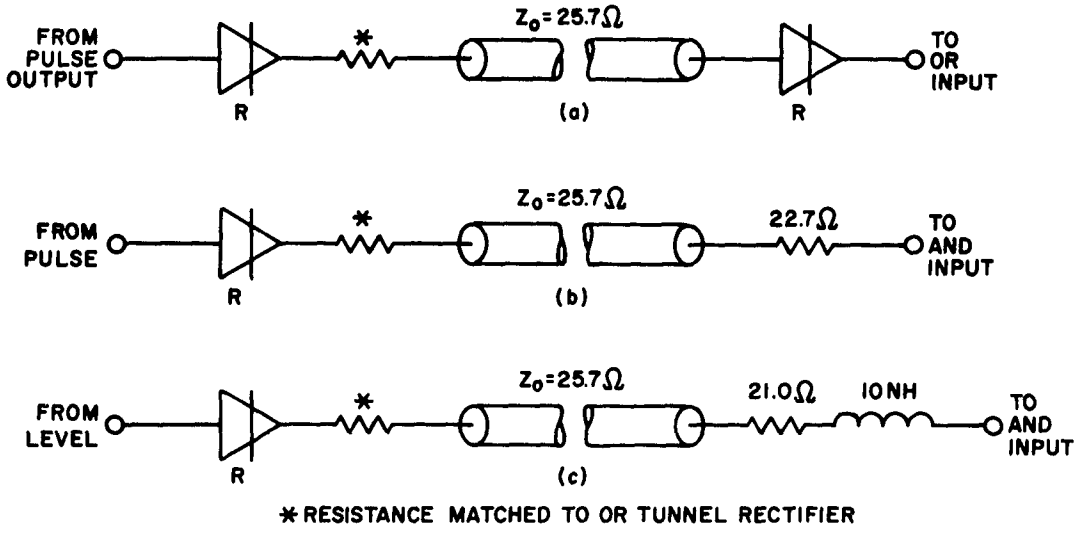


Figure 2-4. Configurations of Special Transmission Line Connections

(j) On the threshold AND gate, part of the input current to TD_1 is available as triggering current of TD_2 (See Figure 2-2). The magnitude of this current is primarily determined by the inductance of the input circuits. It is estimated as shown below:

Pulse Input - 10% of minimum input current

Level Input - 20% of minimum input current

(k) In the design of the output monostable circuit, a safety bias of 1-ma per fan-out is allowed for possible capacitance feedback current. A detailed calculation of capacitance feedback current is given in paragraph 12., Transient Analysis.

9. OR Gate Design (Figure 2-1)

(a) TD_1 (25.5 ma)

(1) Bias Resistance R_1.

$$\frac{6000\ (1 + 0.02)\ -80}{R_1\ (1 - 0.02)} + 0.6 + 0.3 = 25.5\ (1 - 0.02 - 0.05)$$

The equation states that when there is no input, the maximum current through TD_1 should be equal to its minimum peak current after subtracting a 5% safety factor. The first term at the left-hand side is power supply current and the other two terms are the leakage current from the clamping tunnel rectifier and the coupling AND tunnel rectifier, respectively. Thus,

$$R_1 = \frac{6040}{25.5 \cdot 0.93 - 0.9) \cdot 0.98} = \frac{6040}{(23.7 - 0.9) \cdot 0.98}$$

$$= 270 \text{ ohms}$$

(2) Minimum Input Current Required to Trigger TD_1

The difference between the minimum bias current and the current required to drive TD_1 over its peak has to be supplied from the input. The following equation is based on 7% overdrive and taking into consideration possible leakages:

$$i = [25.5(1+0.02+0.07)+0.2+0.5] - \frac{6000\ (1 - 0.02) - 105}{270\ (1 + 0.02)}$$

$$= [27.8 + 0.7] - 21$$

$$= 7.5 \text{ ma}$$

(3) Output Current Available from TD_1 to Supply TD_2

$$i = \frac{6000\ (1 - 0.02) - 300}{270\ (1 + 0.02)} - 0.2 - \frac{1}{9} \cdot 25$$

$$= \frac{5580}{270\ (1 + 0.02)} - 0.2 - 2.8$$

$$= 17.6 \text{ ma, where:}$$

300 mv is assumed to be the output voltage of TD_1 and 0.2 ma is the leakage current at the other input.

(b) TD_2 (51-ma)

(1) Bias Resistance R_2

$$\frac{6000\ (1 + 0.02) - 80}{R_2\ (1 - 0.02)} + 0.7 + 3.0 = 51\ (1 - 0.02 - 0.05), \text{ where:}$$

3.0 ma is the current allowed for capacitance feedback.

$$R_2 = \frac{6040}{(47.5 - 3.7) \cdot 0.98} = \frac{6040}{43.8 \cdot 0.98}$$

$$= 141 \text{ ohms}$$

(2) Minimum Input Current Required to Trigger TD_2

$$i = 51 (1 + 0.02 + 0.07) + 1.0 - \frac{6000 (1 - 0.02) - 105}{141 (1 + 0.02)}$$

$$= 55.6 + 1.0 - 40.1$$

$$= 16.5 \text{ ma, where:}$$

1.0 ma is the greatest leakage current to the two inputs of the AND gates before TD_2 is triggered. Since the current available from TD_1 is 17.6 ma, TD_2 can be properly triggered.

(3) Output Current Available at 450 mv.

$$i = \frac{6000 (1 - 0.02) - 450}{141 (1 + 0.02)} - 0.04 \cdot 51 - 8$$

$$= 37.8 - 2.0 - 8$$

$$= 27.8 \text{ ma, where:}$$

450 mv is chosen as the minimum output voltage. The second term is the current shared by the clamping circuit and the 8 ma is the valley current of TD_2 at 450 mv. The capability of driving three loads is verified by

$$i = 2 (9.7) + 7.7 = 27.1 \text{ ma}$$

which is less than the 27.8 ma of output current from TD_2.

10. Design of Signal Transmission Line Characteristic Impedance

Figure 2-4 shows three different configurations of the signal transmission line termination. The OR tunnel rectifiers at both the sending and receiving ends of the OR gate are primarily to reduce the effect of capacitance feedback. On the other hand, the tunnel rectifier at the sending end of the AND gate will help to reduce the leakage current at low state. Having a resistor at the receiving end of the AND gate instead of a tunnel rectifier gives better tolerance. In other words, the tunnel rectifier at the sending end takes advantage of the desirable non-linear effect at the lower portion of tunnel rectifier curve and the resistor at the receiving end compensates for the undesirable tunnel rectifier characteristic curve at the higher portion. The

characteristic impedance of 25.7 ohms is calculated with the OR tunnel rectifier as termination. At a minimum voltage swing of 345 mv, the current is 7.7 ma which is larger than the 7.5 ma required by the OR gate. The reason for using different resistors at the receiving end of the pulse and the level inputs of the AND gate is to obtain an optimum tolerance design.

The d-c loading curves of the above configurations are plotted in Figure 2-5.

11. AND Gate Design (Figure 2-2)

(a) Threshold AND on TD_1

i_L = Level Input

i_p = Pulse Input

i_b = Bias Current

$\bar{i}$ = Max. Current

$\underline{i}$ = Min. Current

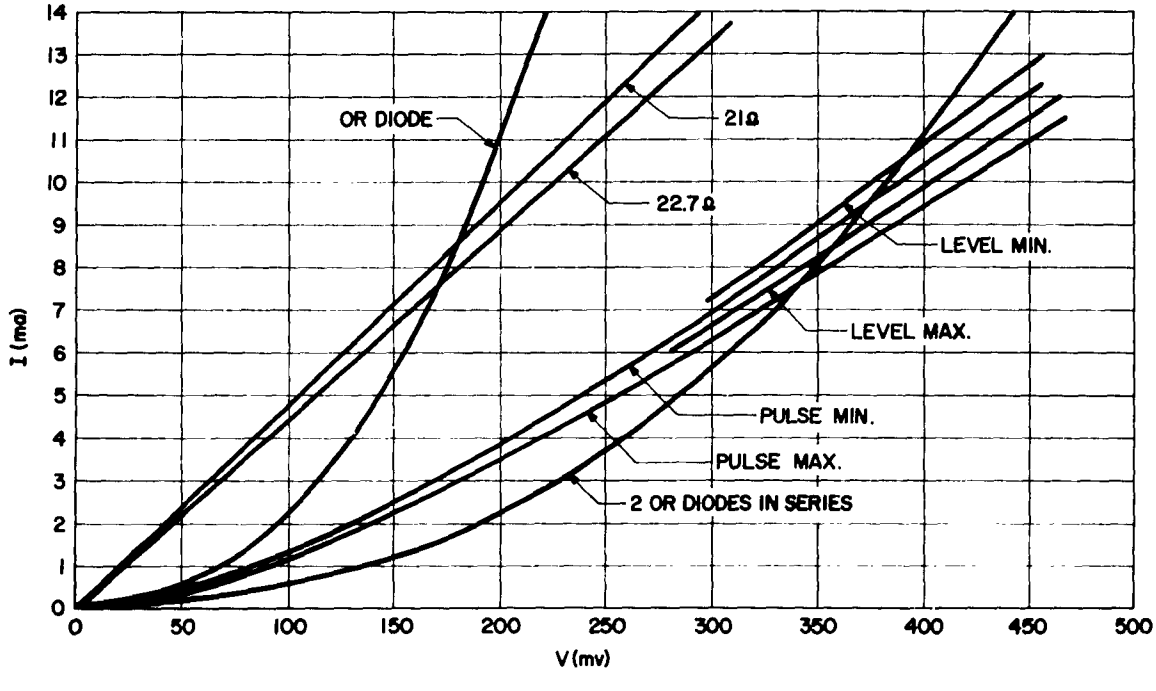


Figure 2-5. Combined Input Loading of AND Gate

(1) Equations (1) and (2) are formulated when there is only one input (TD_1 not triggered).

$$\bar{i}_L + \bar{i}_b \leq (1 - 0.02 - 0.05)\ I_p \qquad (1)$$

$$\bar{i}_p + \bar{i}_b \leq (1 - 0.02 - 0.05)\ I_p \qquad (2)$$

(2) Equation (3) states that when both inputs are high, TD_1 should be triggered.

$$\underline{i}_p + \underline{i}_L + \underline{i}_b \geq (1 + 0.02 + 0.05)\ I_p \qquad (3)$$

(3) The termination resistance of the OR gate should give the same voltage drop as the OR tunnel rectifier.

$$\therefore\ R_p = \frac{170}{7.5} = 22.7 \text{ ohms}$$

$$V_p = 530 - 80 = 450 \text{ mv}$$

From Figure 2-5, $\bar{i}_p = 12.1$ ma

$V_{\underline{p}} = 450 - 105 = 345$ mv

Also from the Figure, $i_{\underline{p}} = 7.7$ ma

(4) $\bar{V}_\ell = 510 - 80 = 430$ mv

For an optimum tolerance design, let

$\bar{i}_\ell = \bar{i}_p = 12.1$ ma

This gives $R_\ell = 21.0$ ohms

$i_\ell = 8.1$ ma

(5) Solve equations (1) and (2) for I_p and i_b with

$\underline{i}_b = 0.96\ i_b$ $\qquad$ $\bar{i}_b = 1.04\ i_b$

$\underline{i}_p = 7.7$ ma $\qquad$ $\bar{i}_p = 12.1$ ma

$\underline{i}_\ell = 8.1$ ma $\qquad$ $\bar{i}_\ell = 12.1$ ma

$$0.96\, i_b = 1.07\, I_p - 15.8$$

$$1.04\, i_b = 0.93\, I_p - 12.6$$

$$I_p = 20 \text{ ma}$$

$$i_b = 5.77 \text{ ma}$$

(6) TD_1 (20 ma)

Bias Resistor $R_1 = 1027$ ohms

(7) Output Current Available from TD_1 to Supply TD_2

$$i = 5.77 \cdot 0.93 - 20\,(\tfrac{1}{9}) + 7.7 \cdot 0.10 + 8.1 \cdot 0.25$$

$$= 5.37 - 2.22 + 0.77 + 2.02$$

$$= 5.94 \text{ ma}$$

The last two terms include the input currents (10% of pulse input and 25% of level input).

(b) TD_2 (20 ma)

(1) Bias Resistance

$$\frac{6000\,(1+0.02) - 80}{R\,(1-0.02)} = 20\,(1-0.02-0.05) - 0.5$$

$$R = \frac{6040}{18.1 - 0.98} = 340 \text{ ohms}$$

(2) Minimum Triggering Current Required

$$i = 20\,(1 + 0.02 + 0.07) - \frac{6000\,(1 - 0.02) - 105}{340\,(1 + 0.02)}$$

$$= 21.8 - 16.7 = 5.1 \text{ ma},$$

which is less than the 5.95 ma that TD_1 can supply.

(3) Current Available from TD_2 to TD_3

$$i = \frac{6000\ (1 - 0.02) - 300}{340\ (1 + 0.02)} = 1/9 \cdot 20$$

$$= 13.88 \text{ ma}$$

(c) TD_3 (35 ma)

(1) Bias Resistance

$$\frac{6000\ (1 + 0.02) - 80}{R(1 - 0.02)} = 35\ (1 - 0.02 - 0.05) - 0.7 - 2.0$$

$$R = \frac{6040}{29.9 \cdot 0.98} = 206 \text{ ohms}$$

(2) Minimum Triggering Required

$$i = 35\ (1 + 0.02 + 0.07) + 1.0 - \frac{6000\ (1 - 0.02) - 105)}{206 \cdot 1.02}$$

$$= 39.2 - 27.5$$

$$= 11.7 \text{ ma},$$

which is less than the 13.8 ma that TD_2 can supply.

(3) Output Current Available at 450 mv

$$i = \frac{6000\ (1 - 0.02) - 450}{206\ (1 - 0.02)} - 0.04\ .35 - \frac{35}{50}\ .08$$

$$= 25.8 - 5.6 - 1.4$$

$$= 18.8 \text{ ma}$$

The capability of driving two loads is verified by

$$i = 7.7 + 9.7 = 17.4 < 18.8 \text{ ma}$$

12. Transient Analysis

A generalized equivalent circuit is shown in Figure 2-6 for the calculation of capacitance coupling current. The formula derived from this equivalent circuit is used in the design of the output stage tunnel diode of the OR and the AND gate.

Given $V(t) = \bar{V}(1 - e^{-\alpha t})$

Then $V(s) = L\left[V(t)\right] = \bar{V}\left(\frac{1}{S} - \frac{1}{S+\alpha}\right) = \frac{\bar{V}\alpha}{S(S+\alpha)}$

And $Z(s) = R_1 + \frac{1}{C_1 S} + \frac{R_2}{R_2 C_2 S + 1}$

$$= \frac{1 + \left[R_2 (C_1 + C_2) + R_1 C_1\right] S + R_1 R_2 C_1 C_2 S^2}{C_1 S (R_2 C_2 S + 1)}$$

$$= \frac{1 + AS + BS^2}{C_1 S (R_2 C_2 S + 1)}$$

Where: $A = R_2 (C_1 + C_2) + R_1 C_1$

$B = R_1 R_2 C_1 C_2$

So,

$$I(s) = \frac{V(S)}{Z(S)} = \frac{\bar{V} \cdot \alpha \cdot C_1 \cdot S (R_2 C_2 S + 1)}{S (S + \alpha) (1 + AS + BS^2)}$$

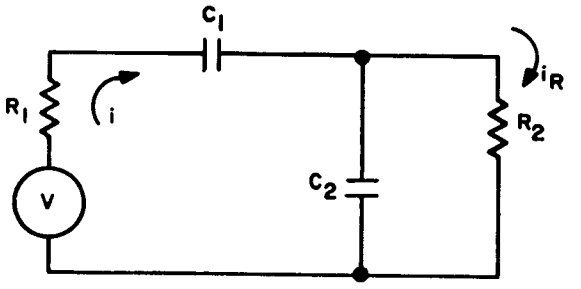


Figure 2-6. Generalized Equivalent Circuit for Calculation of Capacitive Coupling

And $$I_R(S) = \frac{1/C_2 S}{R_2 + 1/C_2 S} \cdot I(S)$$

$$I_R(S) = \frac{V \cdot \alpha \cdot C_1}{(S+\alpha)} \cdot \frac{1}{(1 + AS + BS^2)}$$

Figure 2-7 is an equivalent circuit for the output tunnel diode of an OR gate. Two of the three tunnel diodes connected to this OR gate and being fired at the same time is considered as the worst case.

$\bar{V} = 0.5$ Volt

$\alpha = 1.25 \cdot 10^{10}$ Sec

$C_1 = 2 \cdot \frac{1}{2} = 1 \cdot 10^{-12}$ Farad

$R_1 = 10 \cdot \frac{1}{2} = 5$ Ohms

$R_2 = 6$ Ohms

$C_2 = 10 + 3 + \frac{1}{2} = 13.5 \cdot 10^{-12}$ Farad

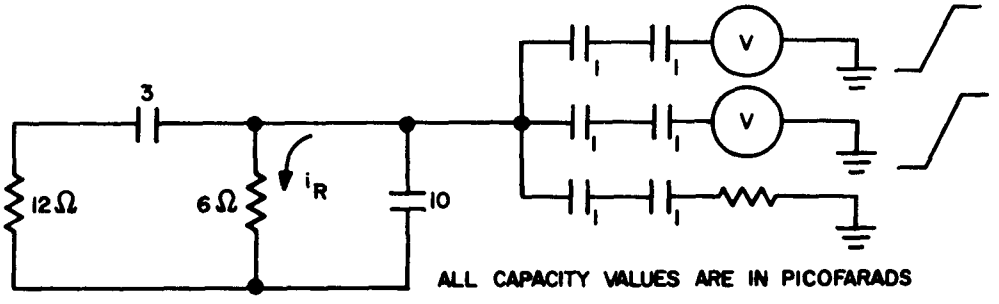


Figure 2-7. Equivalent Circuit of TD_2 of OR Gate

$$\therefore A = \left[R_2 (C_1 + C_2) + R_1 C_1\right]$$

$$= 0.92 \cdot 10^{-10}$$

$$B = R_1 R_2 C_1 C_2$$

$$= 4.05 \cdot 10^{-22}$$

$$I_R(S) = \frac{\overline{V} \alpha C_1}{B} \cdot \frac{1}{(S + \alpha)} \cdot \frac{1}{(S + \gamma)} \cdot \frac{1}{(S + \delta)}$$

Where α, γ, and δ are the roots of the quadric equation

$$S^2 + \frac{A}{B} S + \frac{1}{B} = 0$$

$$S^2 + 2.27 \cdot 10^{11} S + 0.247 \cdot 10^{22} = 0$$

$$S = \left(-1.14 \pm \sqrt{1.29 - 0.247}\right) \cdot 10^{11}$$

$$= (-1.14 \pm 1.04) \cdot 10^{11}$$

$$\therefore \gamma = 1.00 \cdot 10^{10}$$

$$\delta = 21.8 \cdot 10^{10}$$

$$\alpha = 1.25 \cdot 10^{10}$$

And

$$\gamma - \alpha = - 0.25 \cdot 10^{10}$$

$$\delta - \alpha = 20.5 \cdot 10^{10}$$

$$\delta - \gamma = + 20.8 \cdot 10^{10}$$

$$i_R(t) = L^{-1} \left[I_R (S)\right]$$

$$= \frac{\overline{V} \cdot \alpha \cdot C_1}{B} \left[\frac{\epsilon^{-\alpha t}}{(\gamma - \alpha)(\delta - \alpha)} + \frac{\epsilon^{-\gamma t}}{(\alpha - \gamma)(\delta - \gamma)} + \frac{\epsilon^{-\delta t}}{(\alpha - \delta)(\gamma - \delta)}\right]$$

$$= \frac{500 \cdot 1.25}{4.05} \left[\frac{\epsilon^{\alpha t}}{(-0.25)(20.5)} + \frac{\epsilon^{-\gamma t}}{(0.25)(20.8)} + \frac{\epsilon^{-\delta t}}{(-20.5)(-20.8)} \right]$$

$$= 15.4 \left[-1.95\, \epsilon^{-1.25 \cdot 10^{10} t} + 1.92\, \epsilon^{-1 \cdot 10^{10} t} + 0.025 \cdot \epsilon^{-21.8 \cdot 10^{10} t} \right]$$

Approximately,

$$i_R(t) = 15.4 \left[1.92\, \epsilon^{-1 \cdot 10^{10} t} - 1.95\, \epsilon^{-1.25 \cdot 10^{10} t} \right]$$

To avoid tunnel diode triggering by capacitive feedback current, a safety bias equal to maximum $i_R(t)$ should be allowed.

$$\frac{d\, i_R(t)}{d\, t} = 0$$

$$1.92 \cdot \epsilon^{-1.14 \cdot 10^{10} t} - 1.95 \cdot 1.25\, \epsilon^{-1.25 \cdot 10^{10} t} = 0$$

$$t_{max.} = \frac{\text{Log}\ 1.95 \cdot 1.25/1.92}{(1.25 - 1.00) \cdot 10^{10}}$$

$$= \frac{0.24}{0.25} \cdot 10^{-10} = 0.95 \cdot 10^{-10} \text{ sec}$$

$$\therefore\ i_{R/max.} = 15.4 \left[1.92\, \epsilon^{-0.95} - 1.95\, \epsilon^{-1.25 \cdot 0.95} \right]$$

$$= 15.4 \left[\frac{1.92}{2.54} - \frac{1.95}{3.28} \right]$$

$$= 2.5 \text{ ma}$$

B. TUNNEL DIODE AND GATE

1. General

In an effort to overcome the severe d-c tolerance problems of the threshold AND gate, a combination diode-threshold AND gate has been studied. This gate will be referred to as the diode AND gate.

A circuit diagram of the diode AND gate is shown in Figure 2-8. The diodes performing the AND function are: TR_1, TR_3, TR_5, TR_6, TR_7, and TD_3. The AND gate has two inputs designated in Figure 2-8 as terminals 1 and 7. One input is connected to a monostable stage and the other to a bistable stage. The driving stages have two other outputs, each going to other AND gates.

2. Principle of Operation

In order to illustrate the principle of operation, the assumption will be made that the forward resistances of TR_1, TR_3, TR_5, and TR_6 are 18 ohms each, and that there is no conduction in the reverse direction. Consider the current in branch #1. Since the current flowing out of node 3 is fixed by current source I_A (=5ma), the currents, $(I_1 + I_2)$, flowing into node 3 must also be 5 ma. If V_1 is sufficiently lower than V_4, all of I_A is forced to flow through TR_3. If V_1 is sufficiently higher than V_4, all of I_A is forced to flow through TR_1 and I_2 becomes zero. The same reasoning applies to the currents and voltages in branch #2. Figure 2-8 shows the node voltages and currents when both inputs are low (75 mv).

If the bistable stage is switched to the high state, V_7 becomes 450 mv or higher which causes I_5 to become zero. Since the sum of currents at node 4 must be zero and neither I_D nor I_2 can change, I_8 increases from 16 to 21 ma. Similarly, if the monostable stage fires, V_1 becomes 450 mv or higher causing I_2 to become zero. If, however, the voltages out of the bistable and monostable stages are high, I_2 and I_5 become zero, and I_8 increases from 16 to 26 ma. This exceeds the peak current of TD_3, causing it to switch and produce an output.

A good feature of this circuit is that for reliable operation, the input to terminals 1 and 7 need only reach 450 mv. Exceeding 450 mv merely causes TR_3 or TR_5 to go further into cut-off. The accuracy of currents I_2 and I_5 are not controlled by V_1 and V_7 but by the current sources I_A and I_C, which can be maintained within ±4%.

3. Experimental Circuit

The circuit of Figure 2-8 becomes much less attractive when stray circuit elements are considered, in particular the stray capacitors across TR_1, TR_3, TR_5, and TR_6. Fast rising inputs cause sufficient capacitive feedthrough so that the currents are no longer limited sufficiently by the current sources I_A and I_B. In order to investigate this deterioration in performance, five digital computer runs were made. Some of the significant results are presented here.

The equivalent circuit used to study the dynamic behavior of the diode AND gate is shown in Figure 2-9. The expressions for the derivatives of the node voltages are as follows:

$$\frac{d V_1}{d t} = f(t) \quad \left[\text{TABLE}\right]$$

$$\frac{d V_2}{d t} = \frac{1}{C_1}\left[I_1 + C_1 \frac{d V_1}{d t} - \frac{1}{L_2}\int\left(V_2 - V_3\right) d t + K_1\right]$$

$$\frac{d V_7}{d t} = \frac{1}{C_7}\left[I_B - I_7 - \frac{1}{L_5}\int\left(V_6 - V_5\right) d t + K_2\right]$$

$$\frac{d V_6}{d t} = \frac{1}{C_6}\left[I_6 + C_6 \frac{d V_7}{d t} - \frac{1}{L_5}\int\left(V_6 - V_5\right) d t + K_2\right]$$

$$\frac{d V_8}{d t} = \frac{1}{C_9}\left[I_8 - I_9\right]$$

$$\frac{D I_8}{d t} = \frac{1}{L_8}\left[V_4 - V_8 - I_8 R_8\right]$$

$$\frac{d V_4}{d t} = \frac{L_2 L_5 L_8}{L_2 L_5 + L_2 L_8 + L_5 L_8}\left[\frac{1}{L_2}\frac{d v_2}{d t} - \frac{1}{L_2 C_3}\right.$$

$$\left.\left(\frac{1}{L_2}\int\left(V_2 - V_3\right) d t + K_1 + I_3 - I_A\right) + \frac{1}{L_5}\frac{d V_6}{d t}\right.$$

$$\left. - \frac{1}{L_5 C_5}\left(\frac{1}{L_5}\int\left(V_6 - V_5\right) d t + K_2 + I_5 - I_C\right) + \frac{1}{L_8}\frac{d V_8}{d t} + \frac{R_8}{L_8}\frac{d I_8}{d t}\right]$$

$$\frac{d V_3}{d t} = \frac{1}{C_3}\left[\frac{1}{L_2}\int\left(V_2 - V_3\right) d t + K_1 + I_3 - I_A + C_3 \frac{d V_4}{d t}\right]$$

$$\frac{d V_5}{d t} = \frac{1}{C_5}\left[\frac{1}{L_5}\int\left(V_6 - V_5\right) d t + K_2 + I_5 - I_C + C_5 \frac{d V_4}{d t}\right]$$

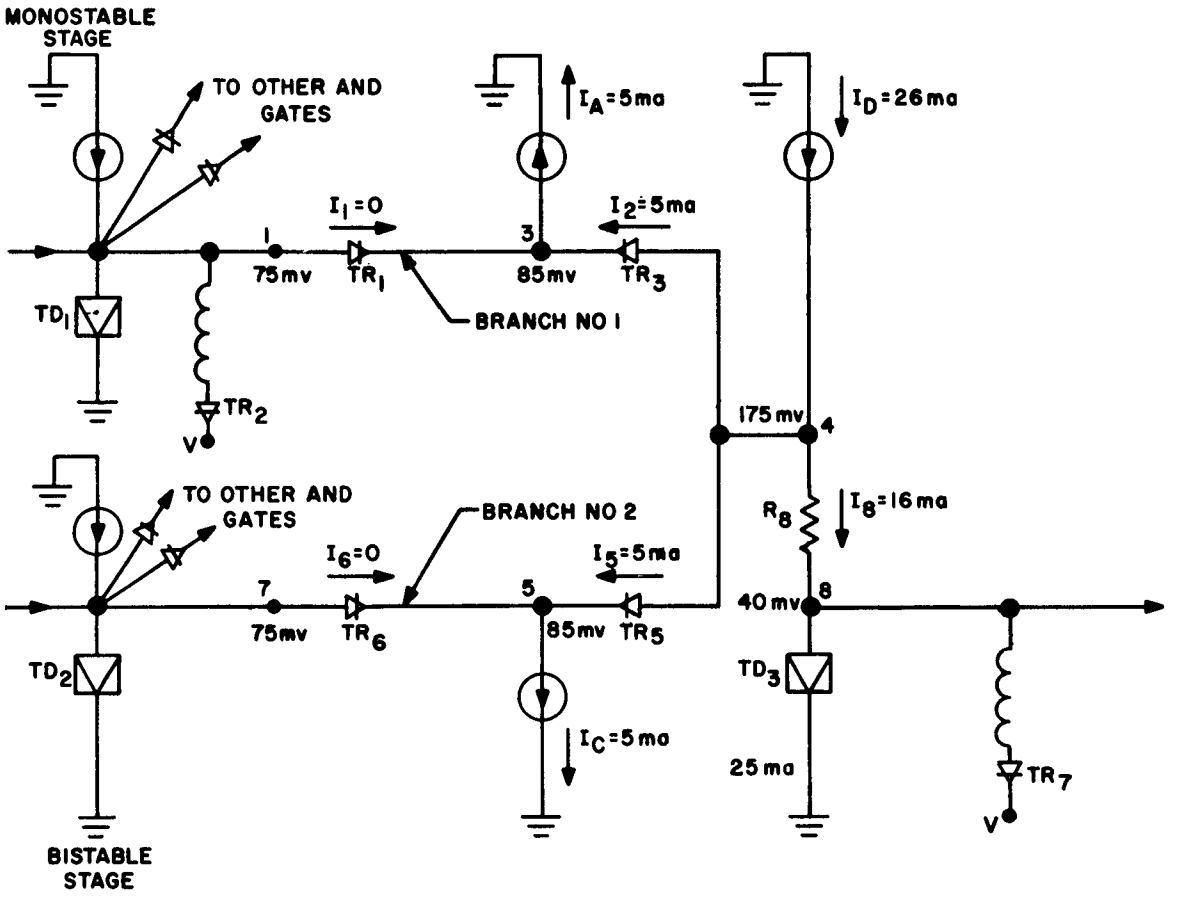


Figure 2-8. Diode AND Gate Circuit

L_2 represents the stray inductances of TR_1 and TR_3; L_5 represents the stray inductances of TR_5 and TR_6; and L_8 represents the stray inductances of R_8 and TD_3.

The currents and voltages shown on the diagram of Figure 2-9 represent initial values.

A Fortran floating-point program was written for this circuit and was compiled and run on an IBM 709 computer. A general flow chart of the program is shown in Figure 2-10. Several runs were also made on an RCA 501.

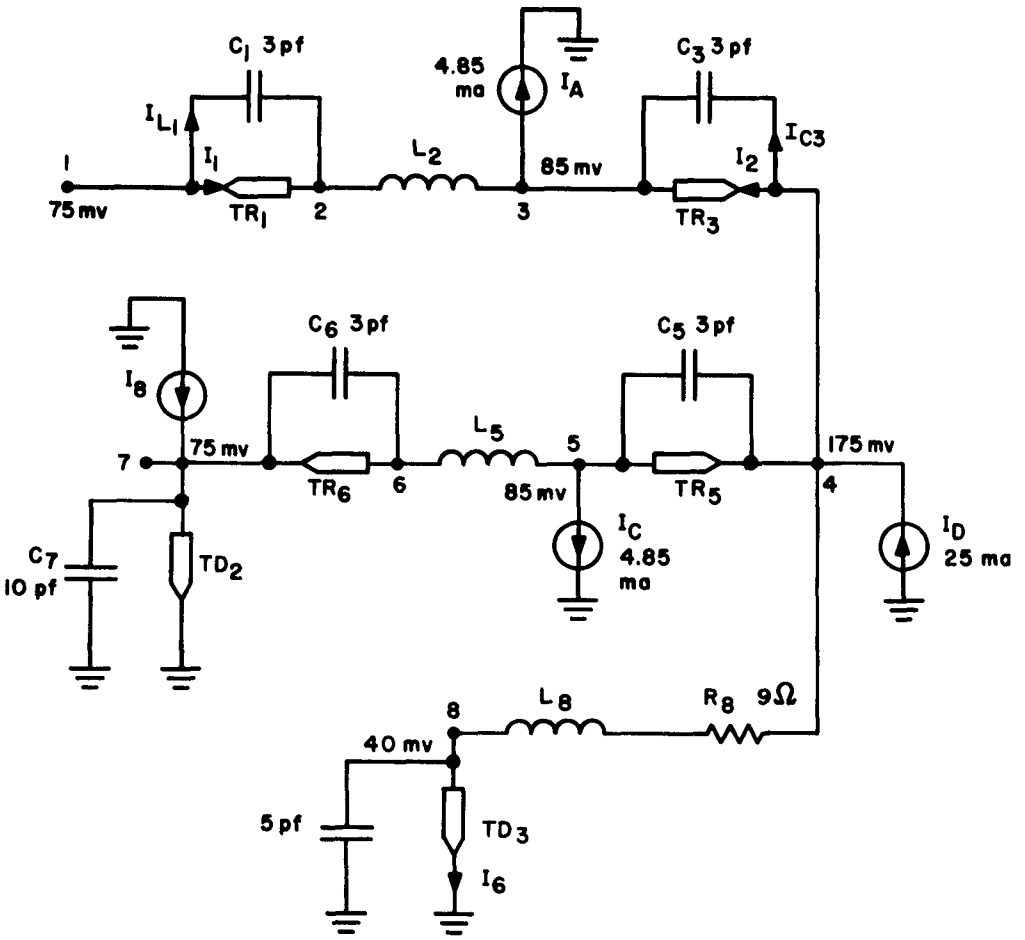


Figure 2-9. Equivalent Circuit of Diode AND Gate used for Computer Runs

A simple iterative technique (described in IRR-10A page 46) was employed in the numerical integration of the equations. If the value of a voltage and its derivative are known at time T, then the voltage at a subsequent time T+H is approximated by the first two terms of a Taylor Series; the value of the integral at time T+H is approximated by the trapezoidal rule. In order to obtain reasonably good accuracy, a time interval, H, of .001 nanosecond was used.

The tunnel-diode characteristics were represented by a table of 25 points and the tunnel-rectifier characteristics by a table of 27 points. A search-and-interpolate routine, using linear interpolation, was used to determine the diode current corresponding to an applied voltage.

The characteristics of the tunnel diodes and tunnel rectifiers are shown in Figure 2-11 and Figure 2-12, respectively.

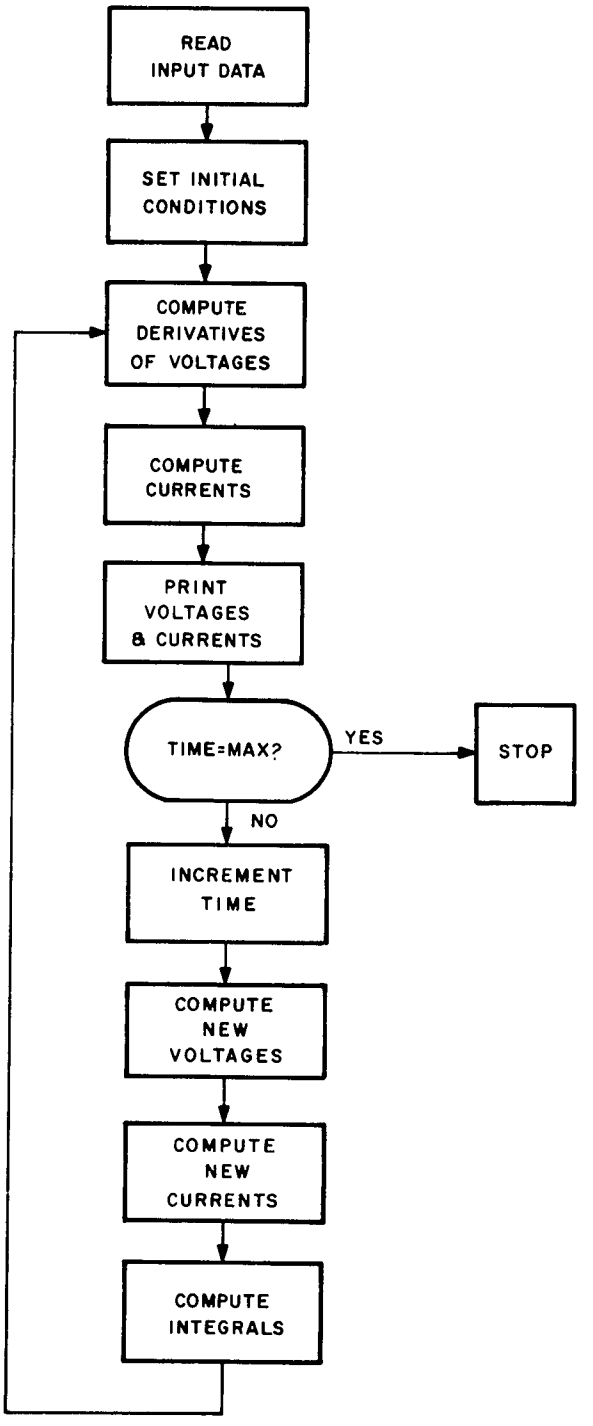


Figure 2-10. General Flow Chart Written for Circuit of Figure 2-9

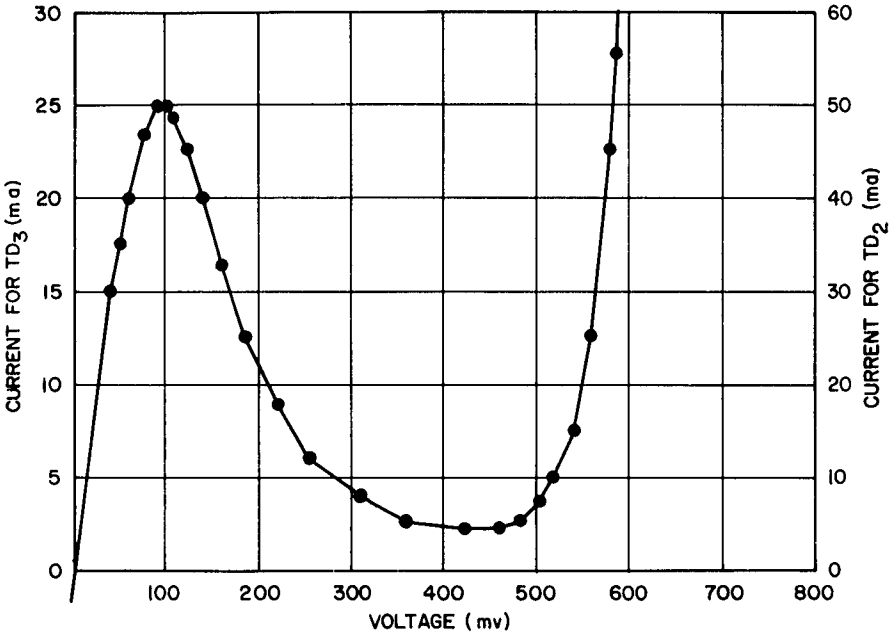


Figure 2-11. Characteristic of Tunnel Diodes used in Circuit of Figure 2-9

All runs were made with the input to terminal 7 low at all times. After 0.1 ns, the time allowed for the circuit to stabilize, a voltage pulse was applied to terminal 1.

To simulate a circuit time of 4 ns, approximately 15 minutes of computer time were required to compile and execute the program. All node voltages and all diode currents were printed for every .01 ns.

Some of the resulting voltage and current waveforms for different inductance and input values are shown in Figures 2-13 to 2-21. It can be seen that in all cases, the capacitive feedthrough causes I_6 to exceed 20 ma, which is the desired current.

Due to this transient feedthrough, this type of AND gate will not be used in the subsystem. However, future work with this type of circuit will continue.

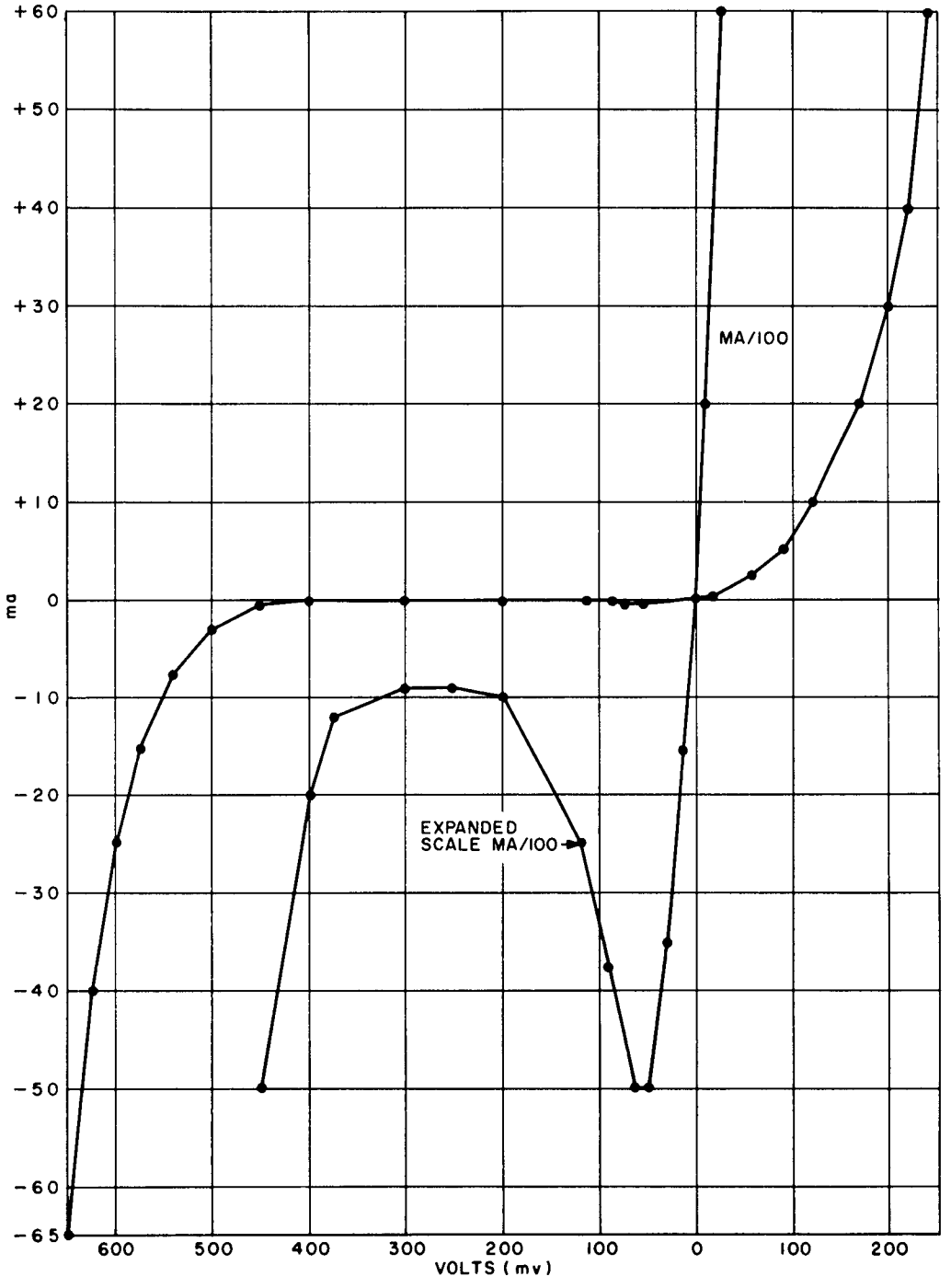


Figure 2-12. Characteristic of Tunnel Rectifiers used in Circuit of Figure 2-9

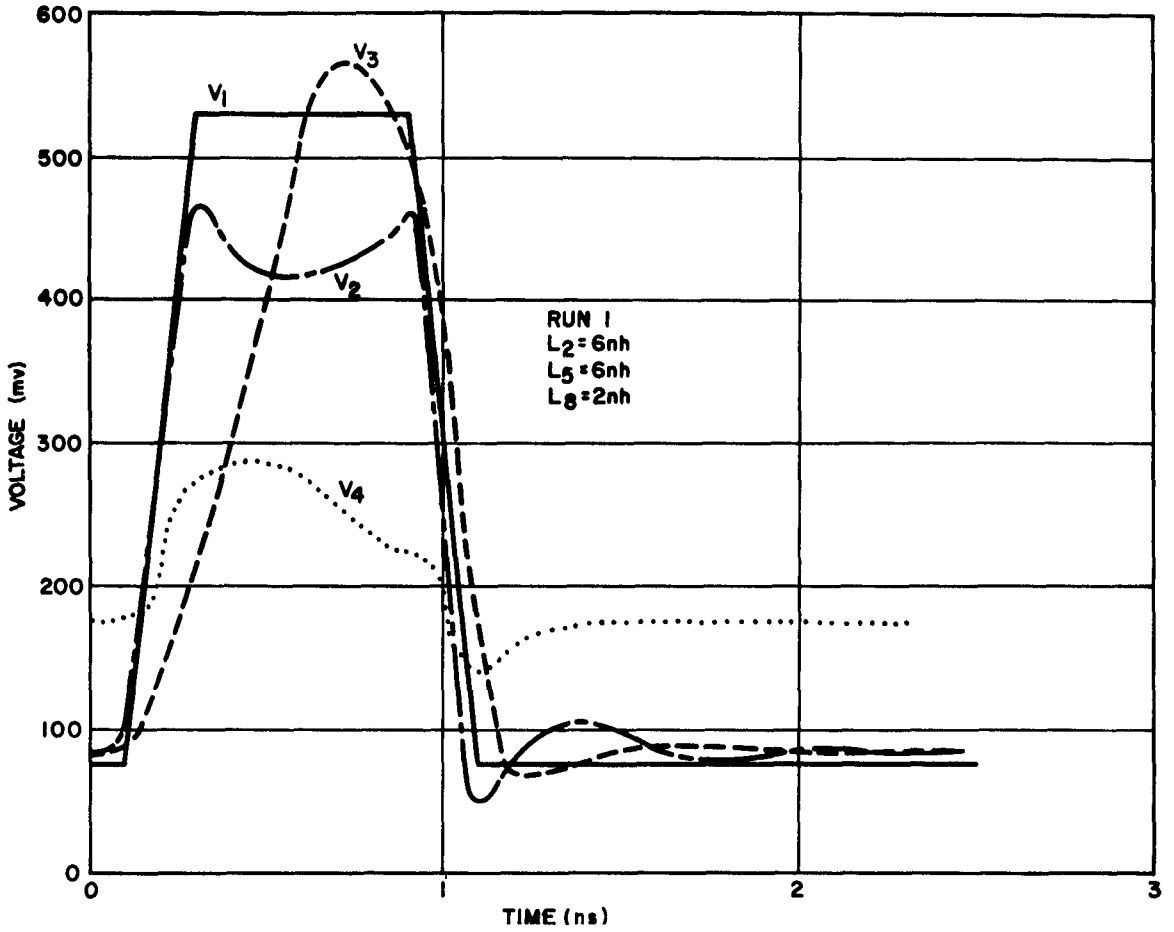


Figure 2-13. AND Gate Voltage Waveforms (Circuit of Figure 2-9)

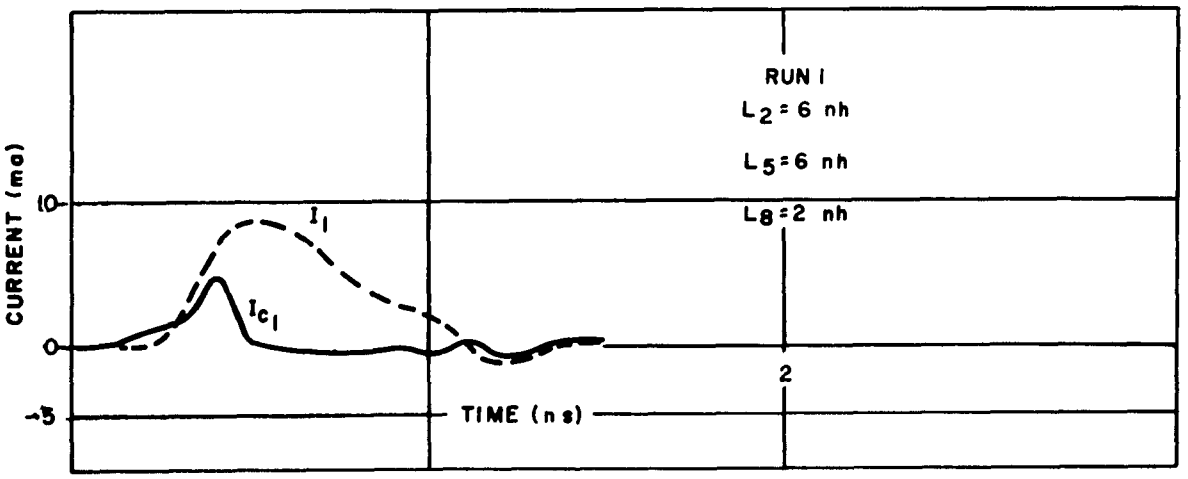


Figure 2-14. AND Gate Current Waveforms (Circuit of Figure 2-9)

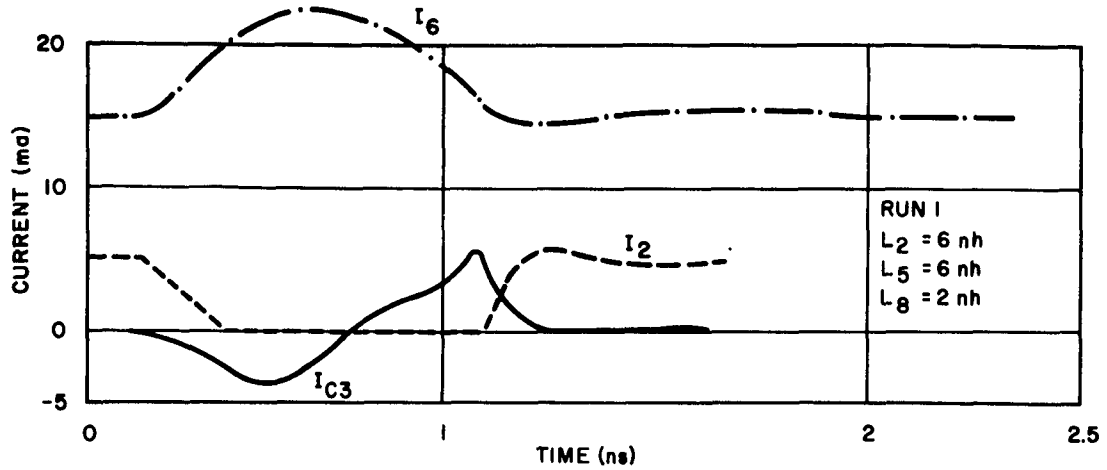


Figure 2-15. AND Gate Current Waveforms (Circuit of Figure 2-9)

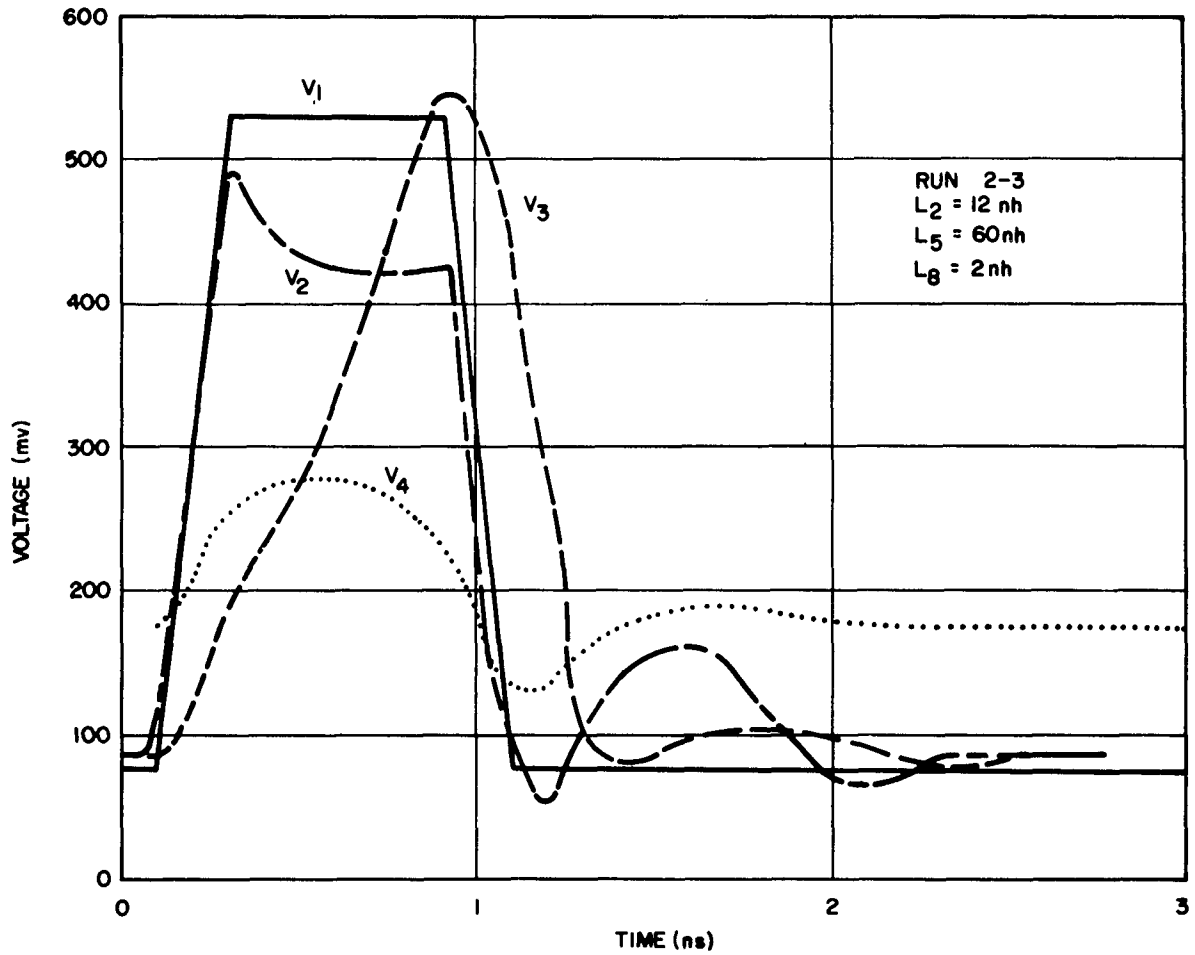


Figure 2-16. AND Gate Voltage Waveforms (Circuit of Figure 2-9)

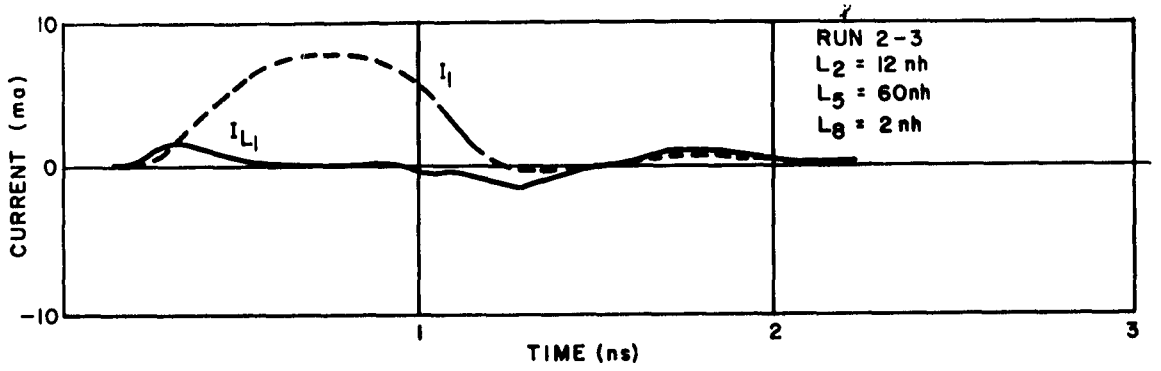


Figure 2-17. AND Gate Current Waveforms (Circuit of Figure 2-9)

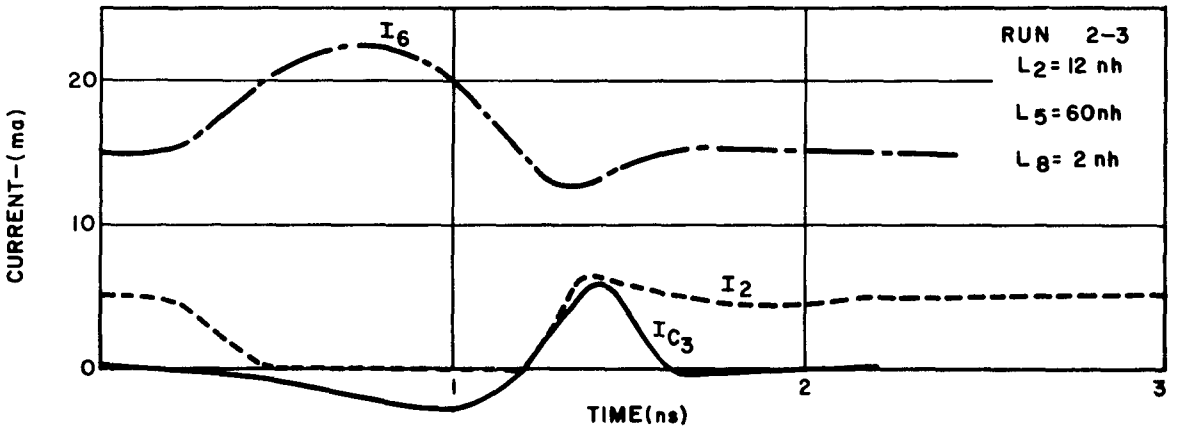


Figure 2-18. AND Gate Current Waveforms (Circuit of Figure 2-9)

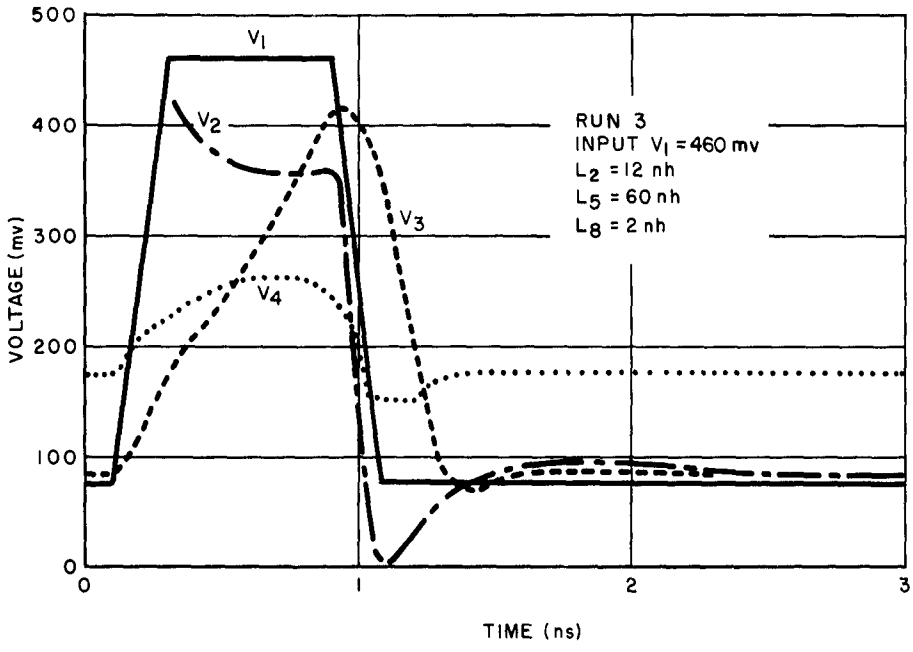


Figure 2-19. AND Gate Voltage Waveforms (Circuit of Figure 2-9)

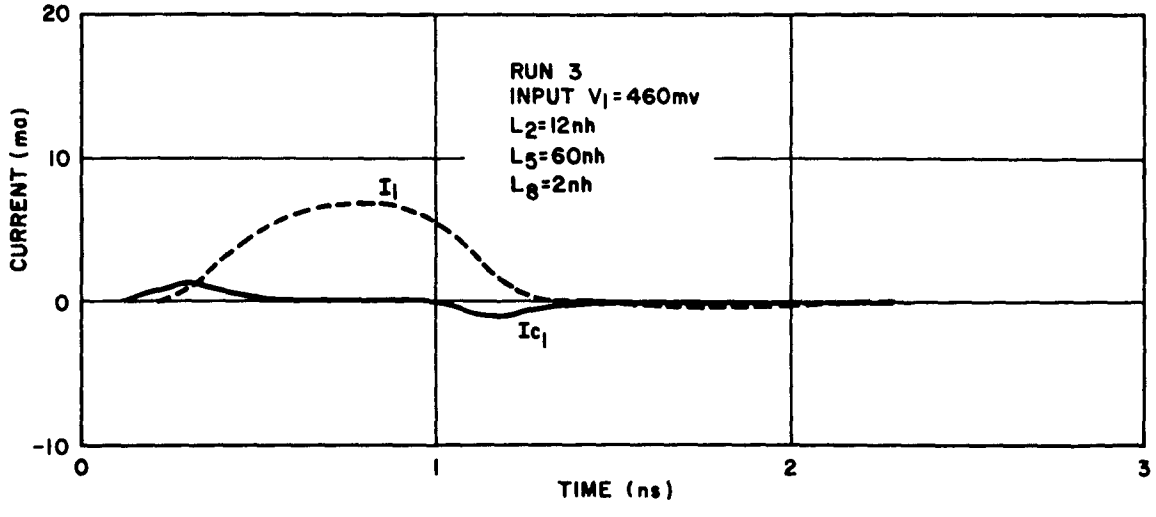


Figure 2-20. AND Gate Current Waveforms (Circuit of Figure 2-9)

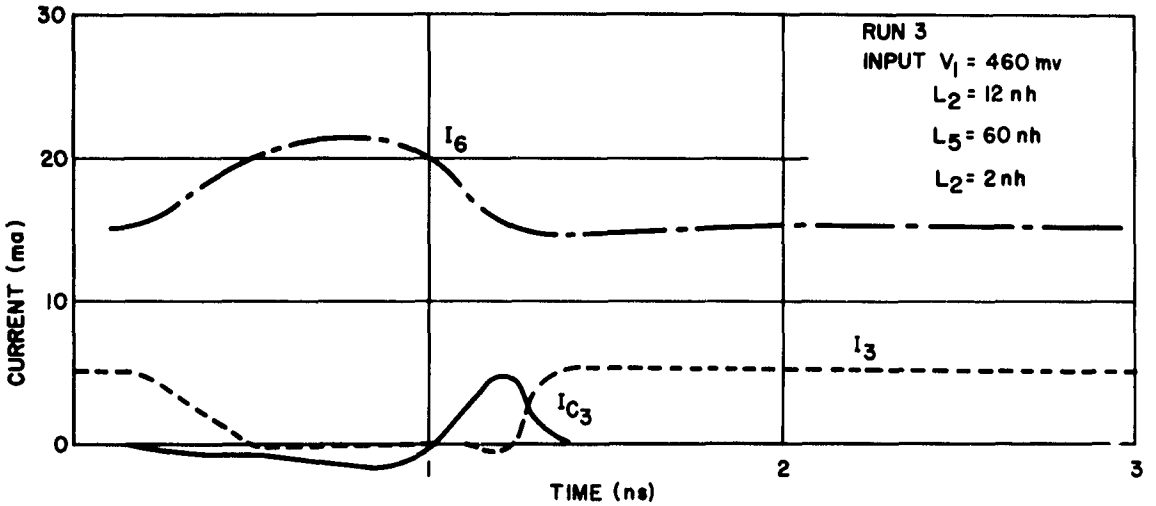


Figure 2-21. AND Gate Current Waveforms (Circuit of Figure 2-9)

C. ANALOG COMPUTER SIMULATION OF MONOSTABLE CIRCUIT

The circuit of Figure 2-22 was simulated on an analog computer by use of the tunnel diode simulation technique discussed in IRR-10A p. 48. In the Figure, each portion enclosed in a dashed line represents a tunneling device (diode or rectifier) together with its stray elements. Each of these diodes has the same configuration and is simulated as shown in Figure 2-23. The area enclosed by broken lines in Figure 2-23 simulates a non-linear element. Potentiometer A is part of the balancing scheme while potentiometer B is used to adjust the peak current of the diode. For example, a 4.2-ma diode is used to simulate a 35-ma diode and R_1 and R_2 can have odd values. Potentiometer C is used to subtract, from the characteristic of the physical diode used, its stray resistance so that the proper amount can be added by potentiometer D for the diode simulated. Figure 2-24 shows the complete simulation where each box refers to a scheme such as Figure 2-23; the number in the box refers to the encircled number in Figure 2-22.

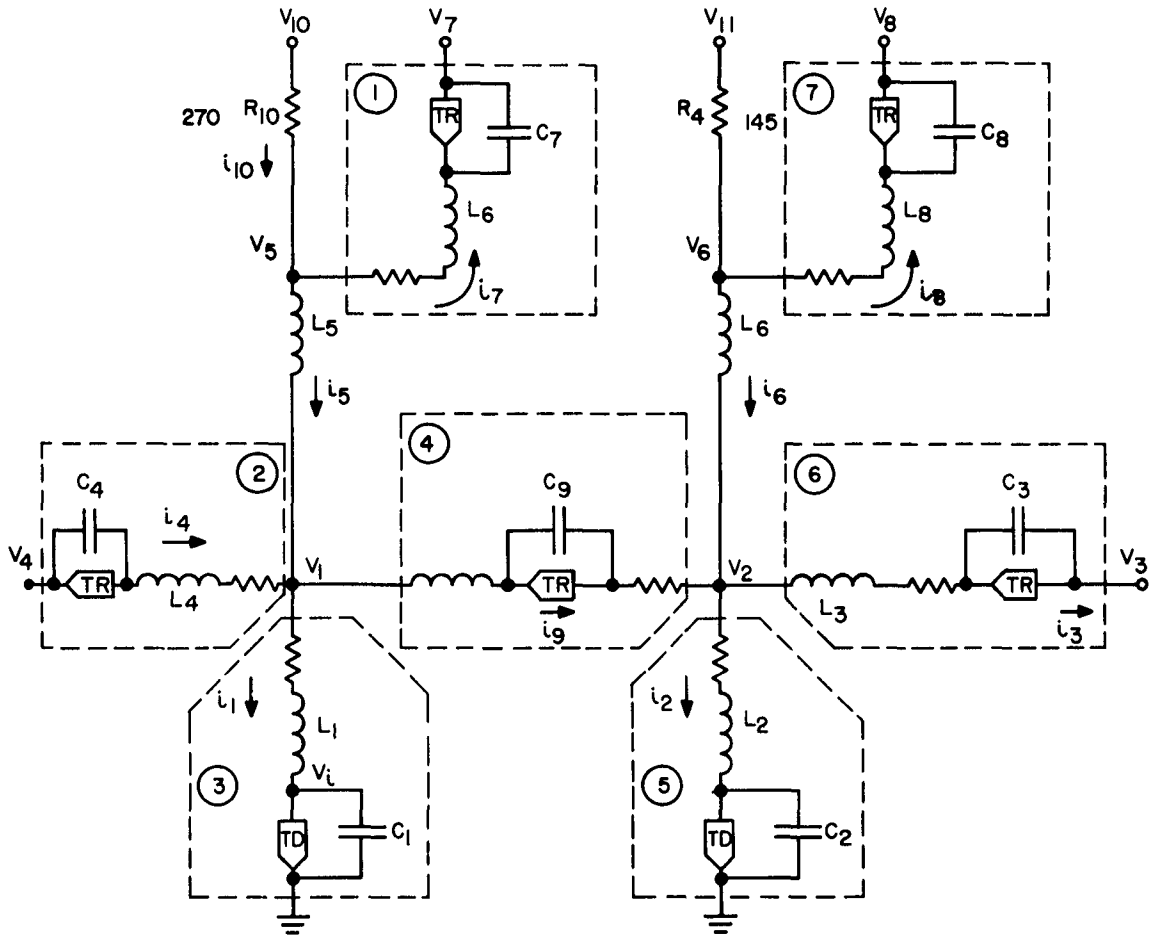


Figure 2-22. Model of Monostable Circuit

All diodes except No. 6 have nominal characteristics, nominal values of capacitance and series resistance, as well as a series inductance of 1 nh. The current-voltage scale of diode No. 6 was changed to represent a parallel combination of 3 branches of the series connection of AND and OR diodes.

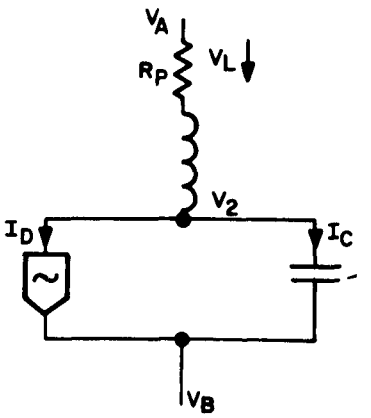


Figure 2-23a. Model of Tunneling Device

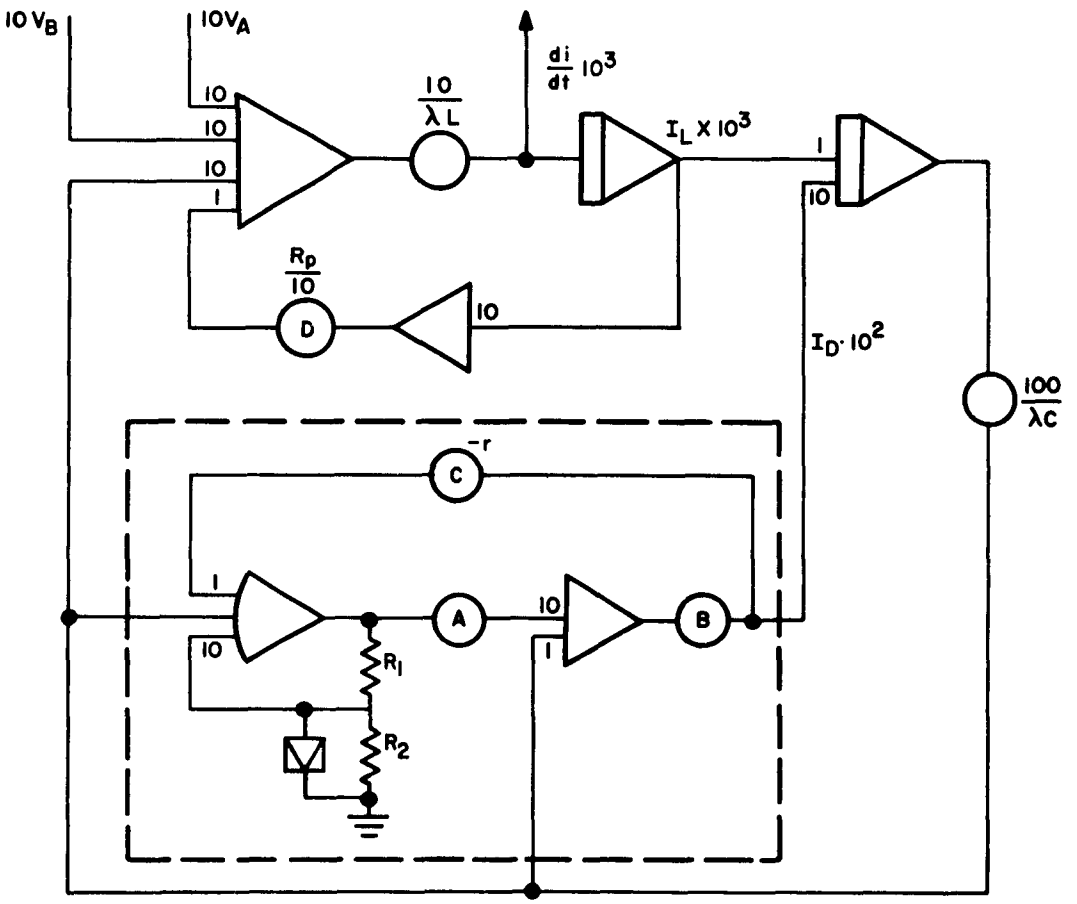


Figure 2-23b. Simulation of Circuit of Figure 2-23a

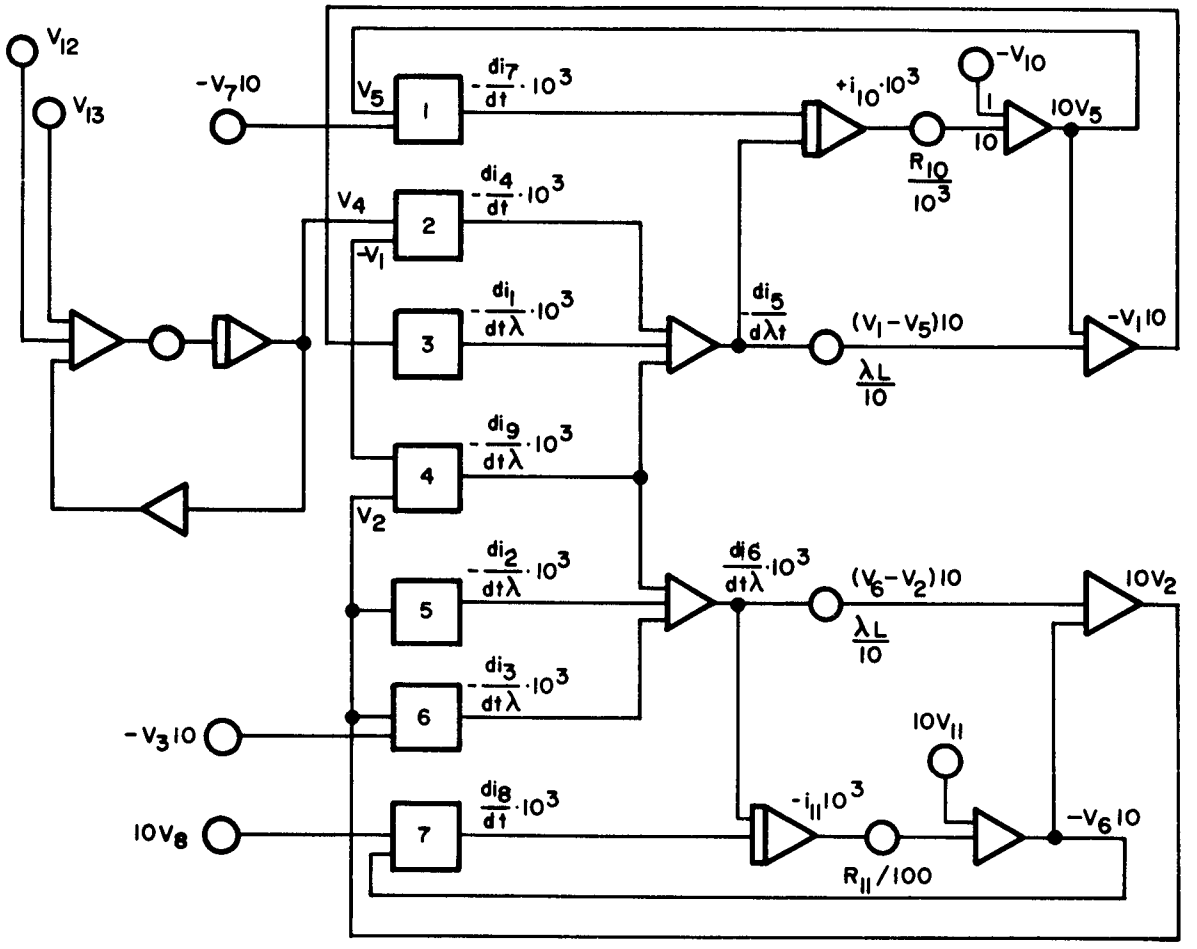


Figure 2-24. Simulation of Circuit of Figure 2-22

The simulation is straightforward except for one point: the nodal equations at V_1 and V_2 (Figure 2-22) are written not for the current, but for its time derivative, $\Sigma\, di/dt = 0$. This is because all branches coming into these nodes are composed of elements (tunnel diodes and inductances) that require, in simulation, obtaining current from voltage and not vice versa. Hence, to be able to use the nodal equation the voltage on L_5 is found from di/dt.

The time scale factor was 10^{10}; the current and voltage scales are shown in the schematics.

This simulation, which contained seven non-linear elements, shows the feasibility of the simulation method using tunnel diodes. It was found that the holder arrangement (consisting of R_1, R_2 and the diode in Figure 2-23b) withstood considerable overload when R_1 was a metal film resistor. The various voltages and currents were recorded on a channel recorder, while x-y plots were also made of i_1 vs. v_1' and C_2 vs. V_2'.

Figures 2-25 and 2-26 show the waveforms of computer runs 15 and 16 while Figures 2-27 and 2-28 show the respective switching trajectories. The operating conditions for both circuits are the same; only for run 16, the load is disconnected. These two runs simulated the circuit under normal operating conditions, and the results are in accordance with laboratory observations and theoretical assumptions.

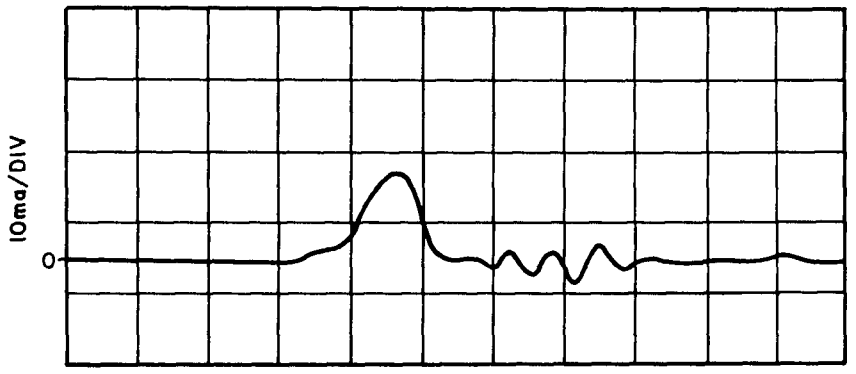
Another experiment was performed which consisted of applying a train of pulses to the circuit input. The separation between the pulses was progressively decreased. The total pulse period was found by determining the minimum operation which still produced an output pulse. The period was found to be 3.5 ns for inductances of 10 and 5 nh and 2.6 ns for inductances of 6 and 3 nh.

A different experiment was made which consisted of reversing the polarity of the coupling diodes between the stages and finding how high the second stage has to be biased in order to be triggered by the capacitive coupling. Under this condition the situation is similar to that of Figure 2-29 where circuit A triggers OR circuit B and circuit B must not backtrigger circuit C through the diode capacitance. It was found that the diode of circuit 2 had to be biased 1 to 2 ma from the peak in order for triggering to occur.

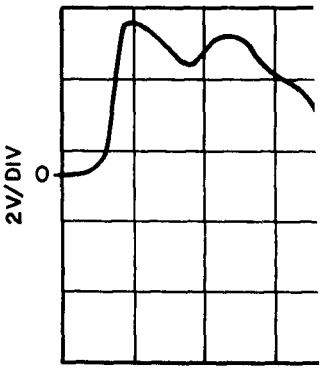
Still another experiment was performed by lowering the current in R_{10}, increasing inductance L_4 to about 12 nh and increasing the input. This condition simulates the case of an AND circuit where it is wished to utilize, by virtue of the large L_4 inputs, available current to drive the second stage. Figure 2-30 shows the various waveforms obtained by this experiment.

D. BISTABLE CIRCUIT

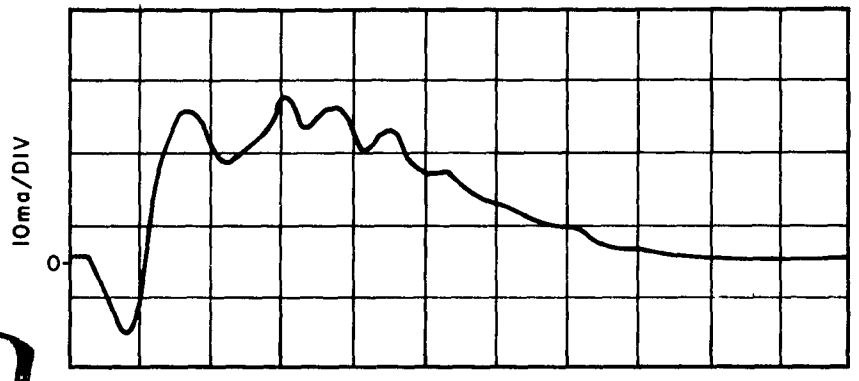
This circuit was described in the supplement to IRR-10A pg. S-74 to S-77, and has been chosen for use in the logic subsystem. The circuit may be set or reset with a positive pulse. Two such bistables will make-up a flip-flop, capable of operating at a 100-mc repetition rate.



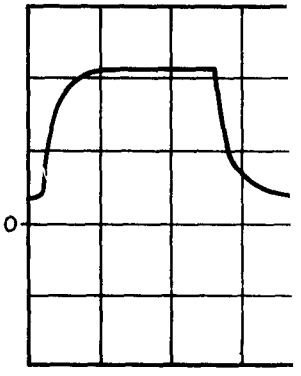
I_9 .2 NANOSECOND / DIV



V_1'



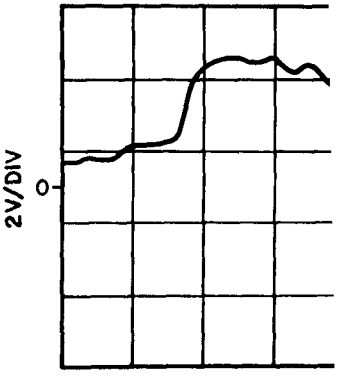
I_1 .2 NANOSECOND / DIV



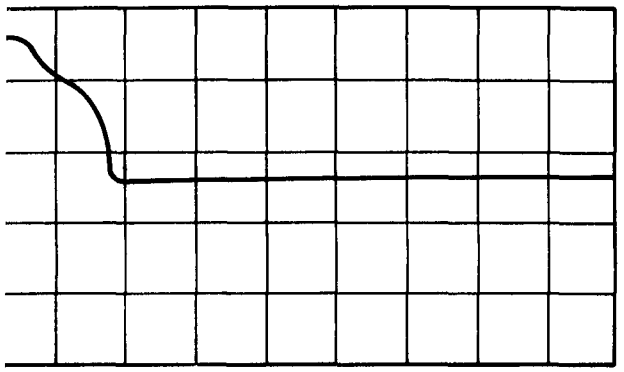
INPUT .2

1

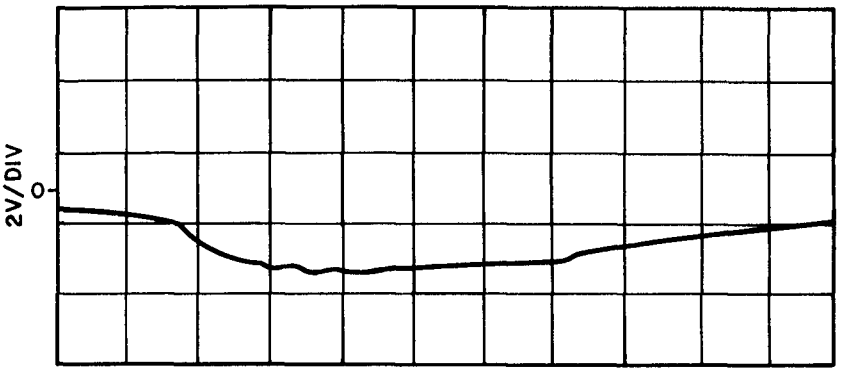
V_1 .2 NANOSECOND / DIV



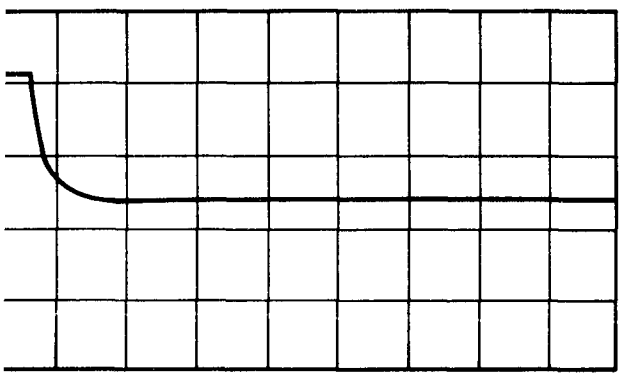
V_2 .2



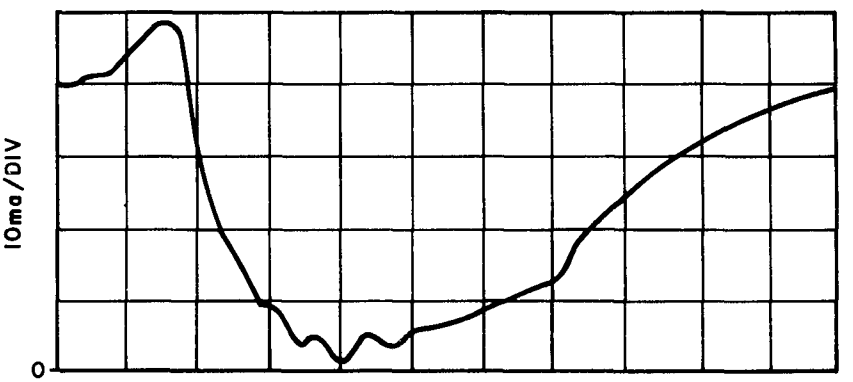
.2 NANOSECOND / DIV



V_6 .2 NANOSECOND / DIV



.2 NANOSECOND / DIV



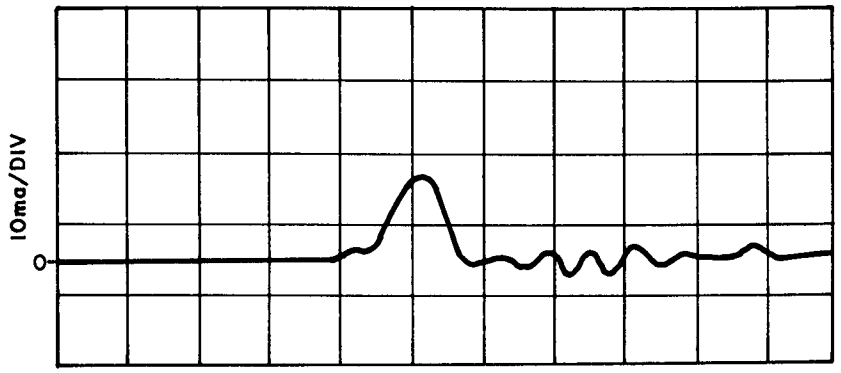
I_2 .2 NANOSECOND / DIV

.2 NANOSECOND / DIV

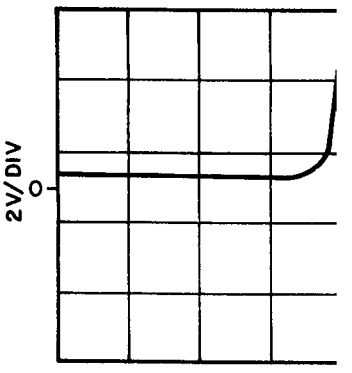
I_3 .2 NANOSECOND / DIV

2

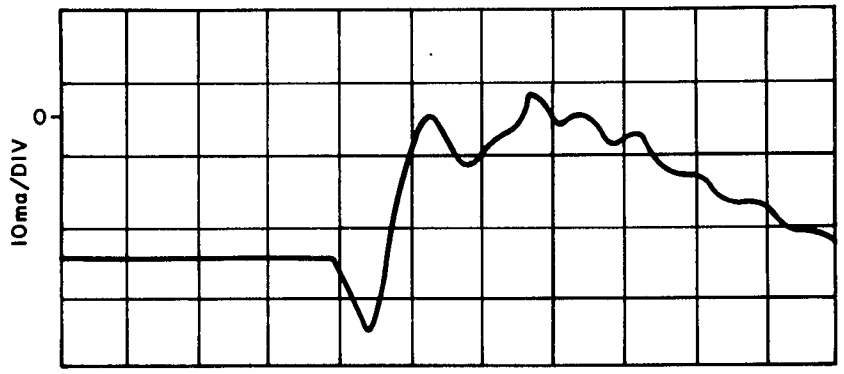
Figure 2-25. Waveforms of Computer Run 15



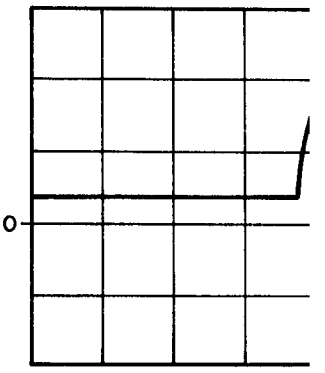
I_9 2 NANOSECOND / DIV



V_1' .2



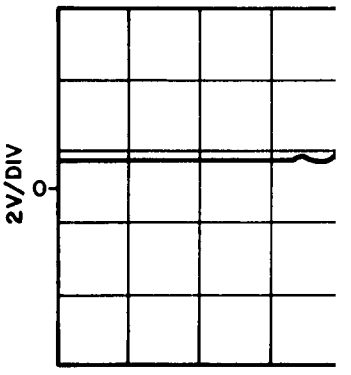
I_1 .2 NANOSECOND / DIV



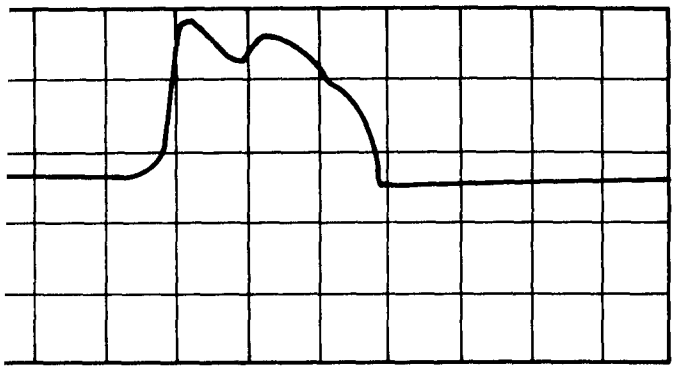
INPUT .2

1

V_1 2 NANOSECOND / DIV

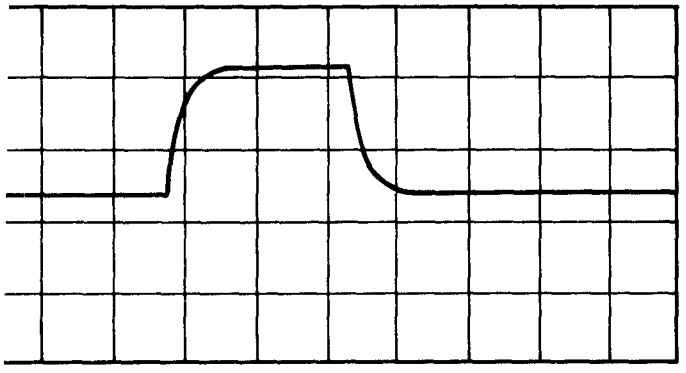


V_2 .2



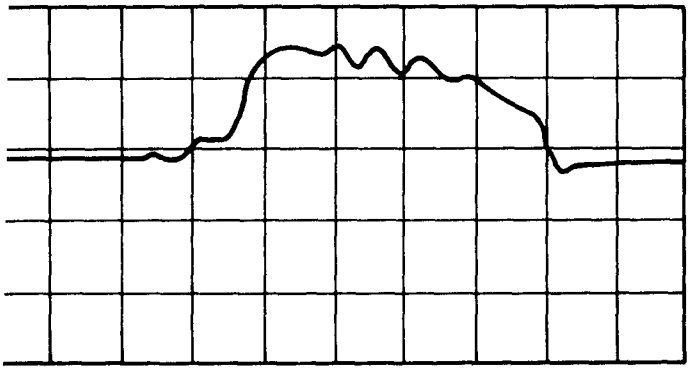
.2 NANOSECOND / DIV

V_6 .2 NANOSECOND / DIV

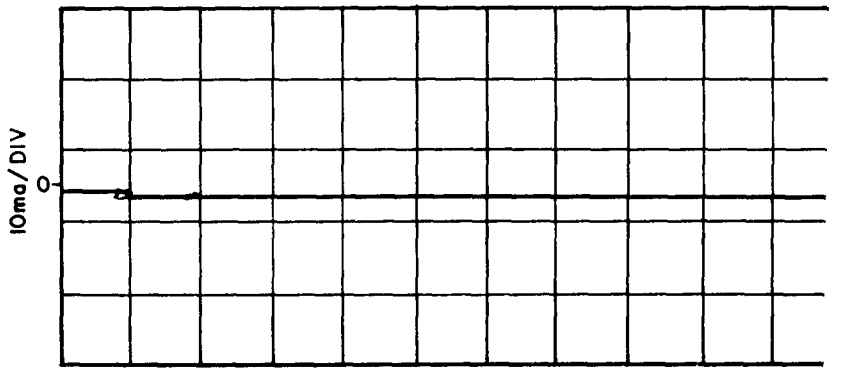


.2 NANOSECOND / DIV

I_2 .2 NANOSECOND / DIV



.2 NANOSECOND / DIV



I_3 .2 NANOSECOND / DIV

2

Figure 2-26. Waveforms of Computer Run 16

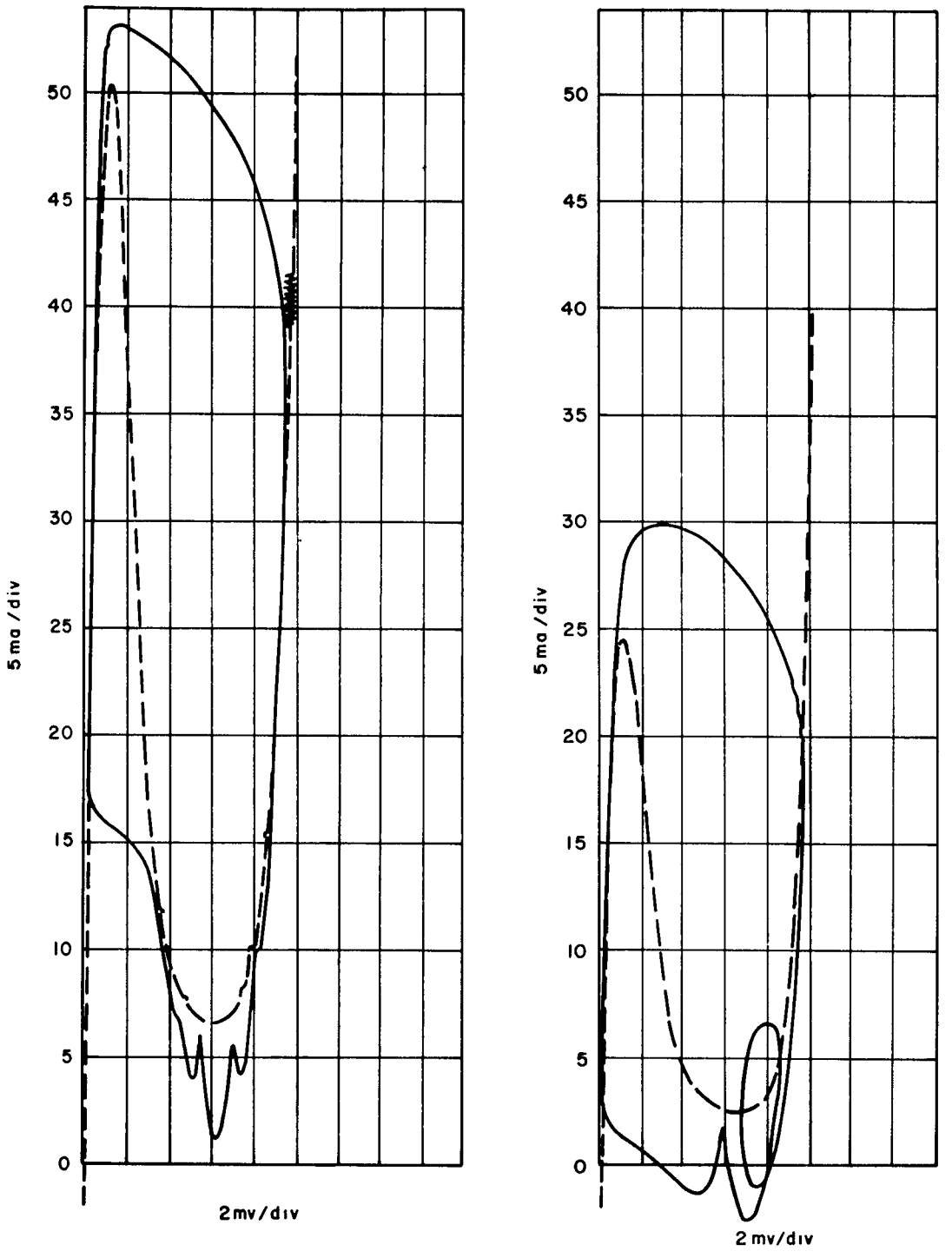


Figure 2-27. Switching Trajectory for Computer Run 15

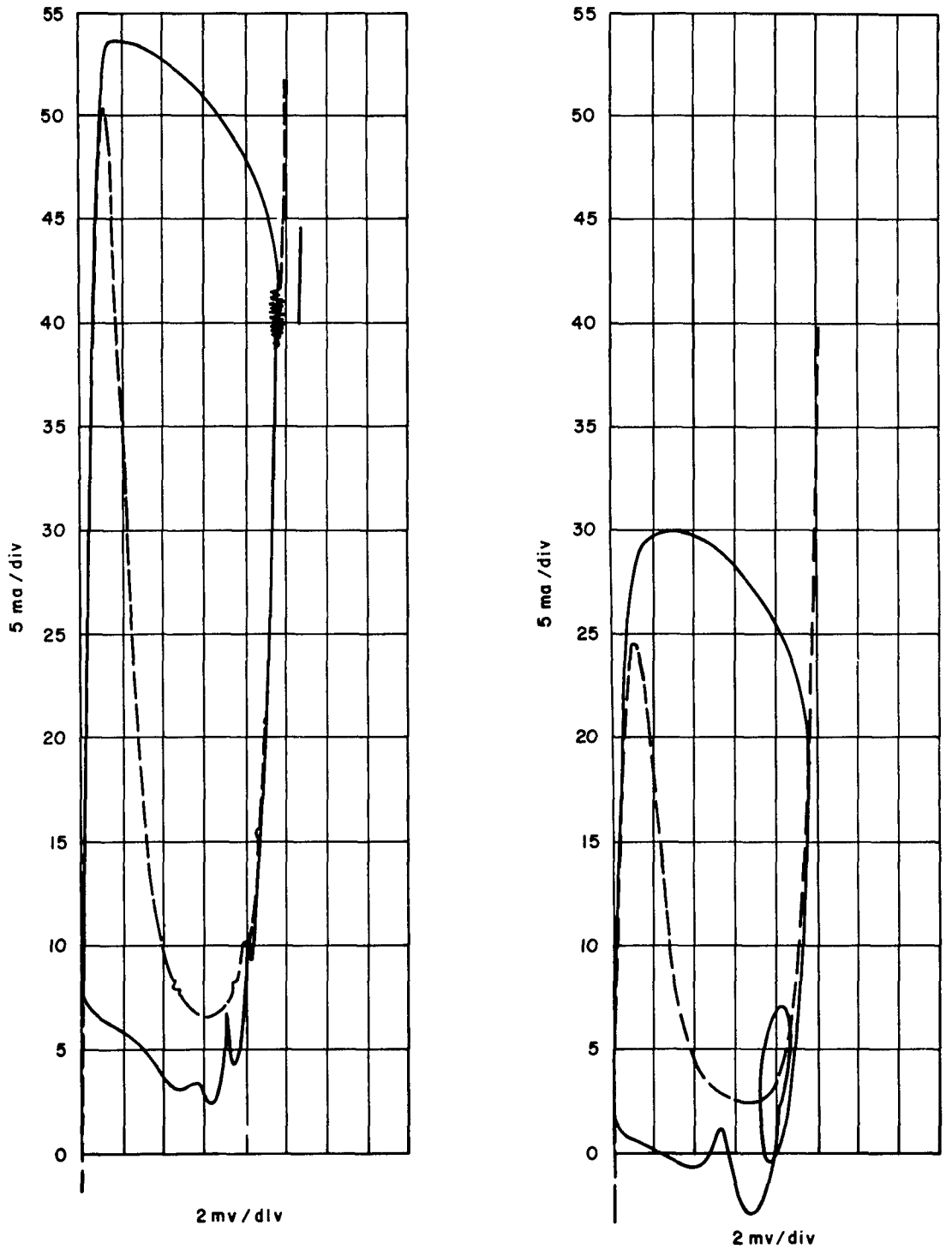


Figure 2-28. Switching Trajectory for Computer Run 16

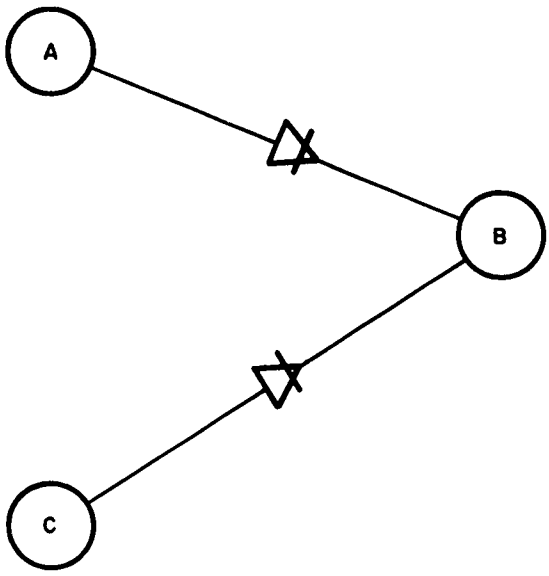


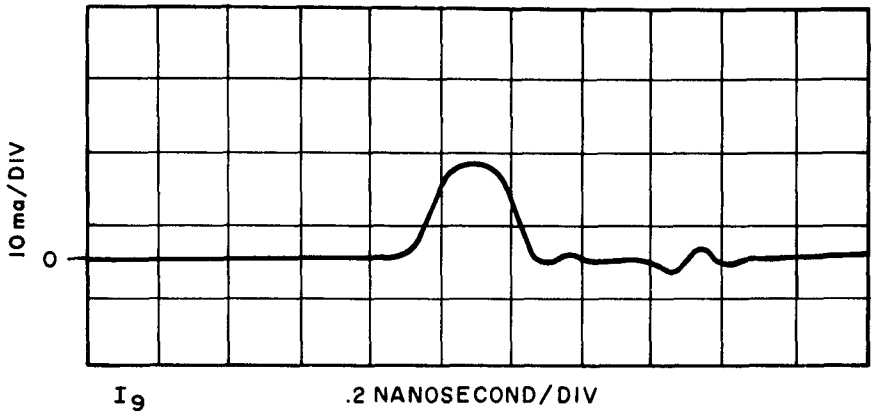
Figure 2-29. Configuration of OR Circuit where Backtriggering Could Occur

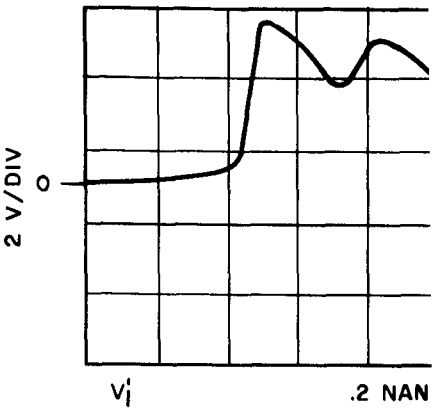
This report describes the principle of operation and provides a guide for optimum, reliable design. Included herein is a dynamic and static tolerance analysis, switching trajectories, a complete circuit diagram and a set of typical waveforms at various points of the circuit.

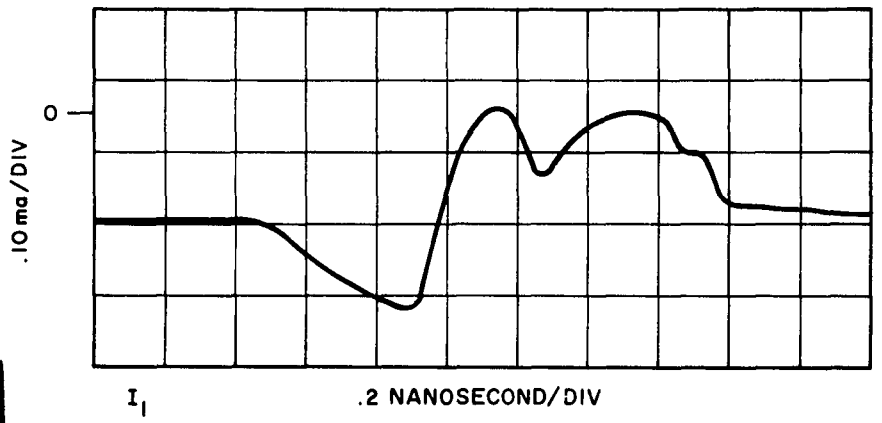
1. Principle of Operation

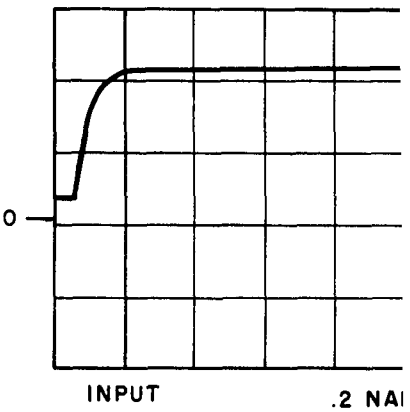
The bistable circuit may be divided into a number of blocks performing various functions, as illustrated by the block diagram in Figure 2-31. Only one block on this diagram is bistable, the others are monostable and their only function is to switch the bistable unit to its "high" or "low" state via the available set and reset inputs. The set and reset inputs are positive pulses. Any one of the set inputs is amplified by the "set amplifier" which switches the "bistable unit" to its high voltage state. This represents a "1". Any one of the reset inputs switches the "inverter driver" which activates the "inverter" to produce a negative pulse. This negative pulse switches the bistable unit to its low voltage state, representing a "0".

In order to illustrate the operation principle of the bistable circuit, a simplified circuit diagram will be considered. This circuit is shown in Figure 2-32. Here some of the stray reactive elements have been omitted. The circuit is divided into parts corresponding to those on the block diagram of Figure 2-31.

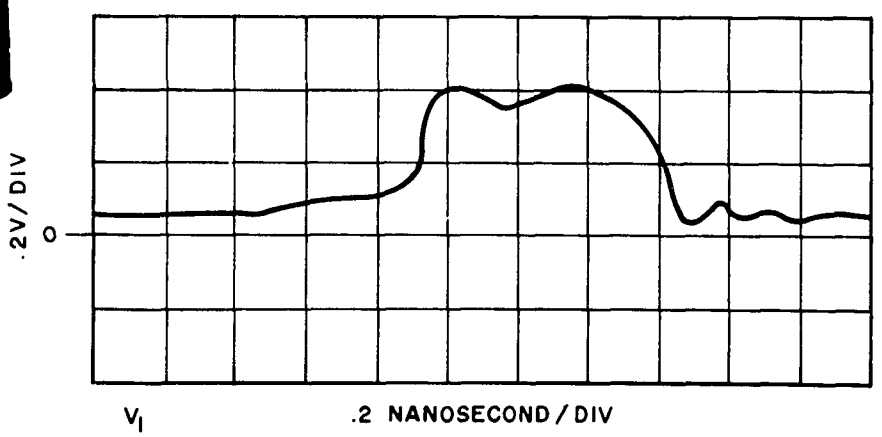

10 ma/DIV
0
I_9
.2 NANOSECOND/DIV

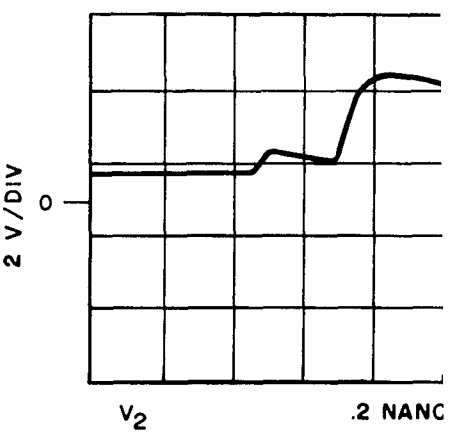

2 V/DIV
0
V_1'
.2 NAN

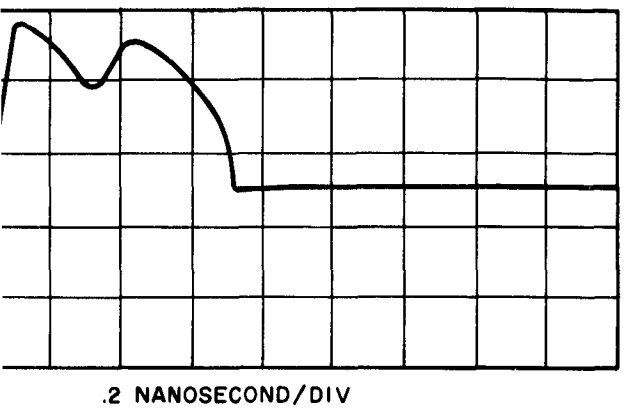

.10 ma/DIV
0
I_1
.2 NANOSECOND/DIV

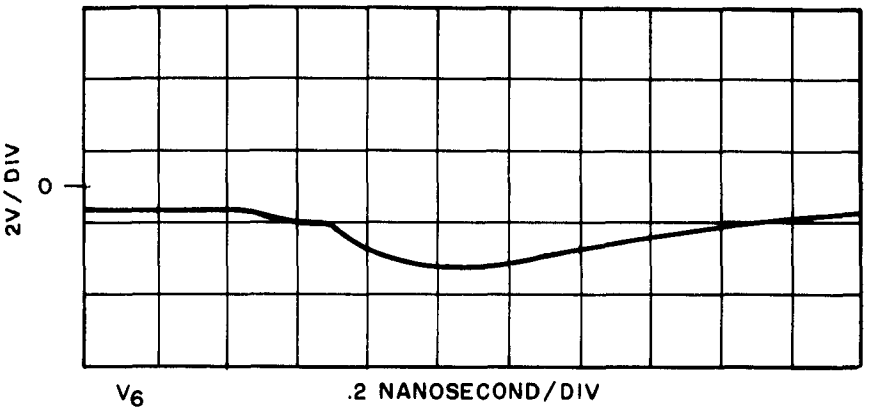

0
INPUT
.2 NAI

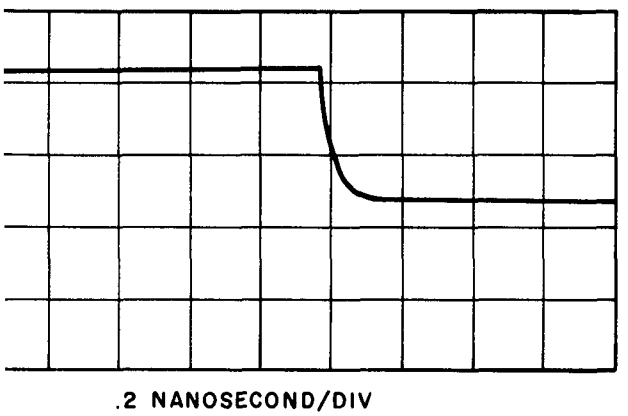
1

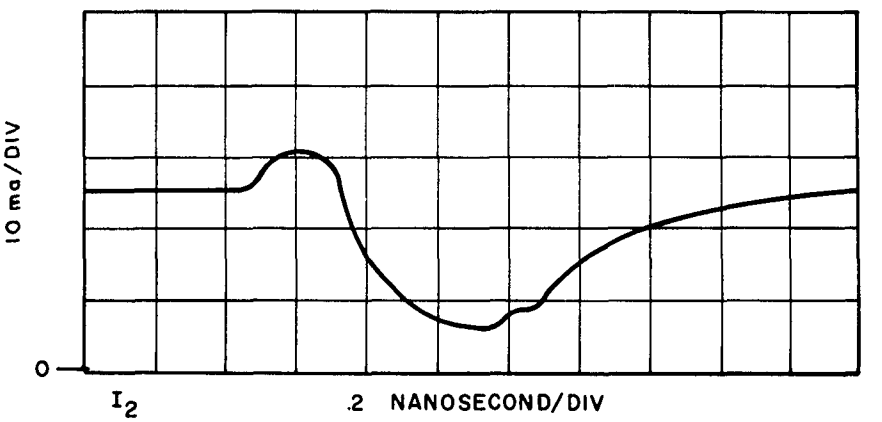

.2V/DIV
0
V_1
.2 NANOSECOND/DIV

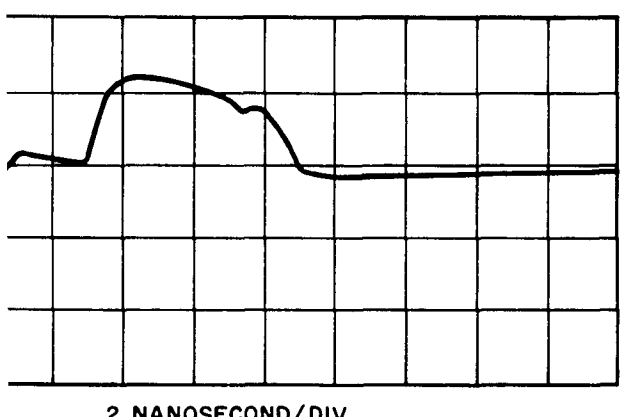

2 V/DIV
0
V_2
.2 NANO

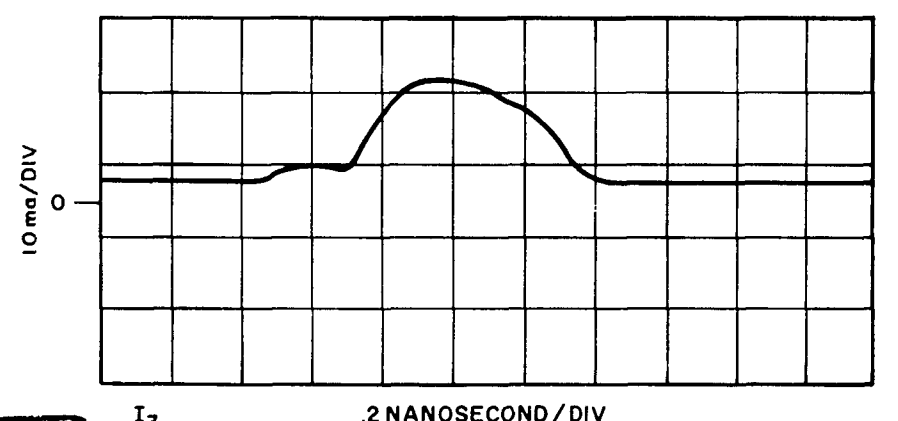












2

Figure 2-30. Waveforms of Computer Run 32

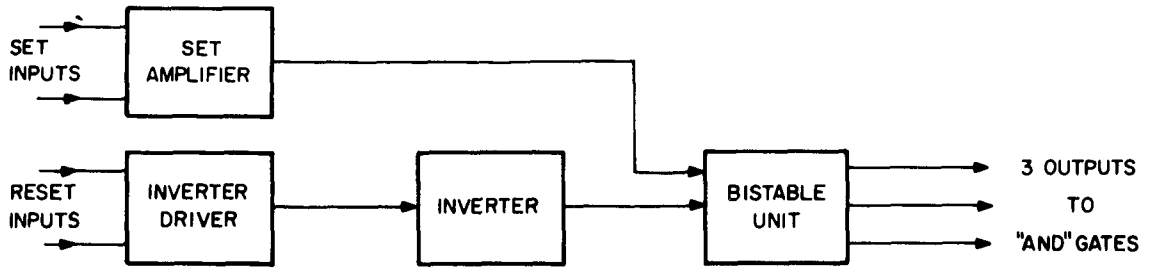


Figure 2-31. Block Diagram of Bistable Circuit

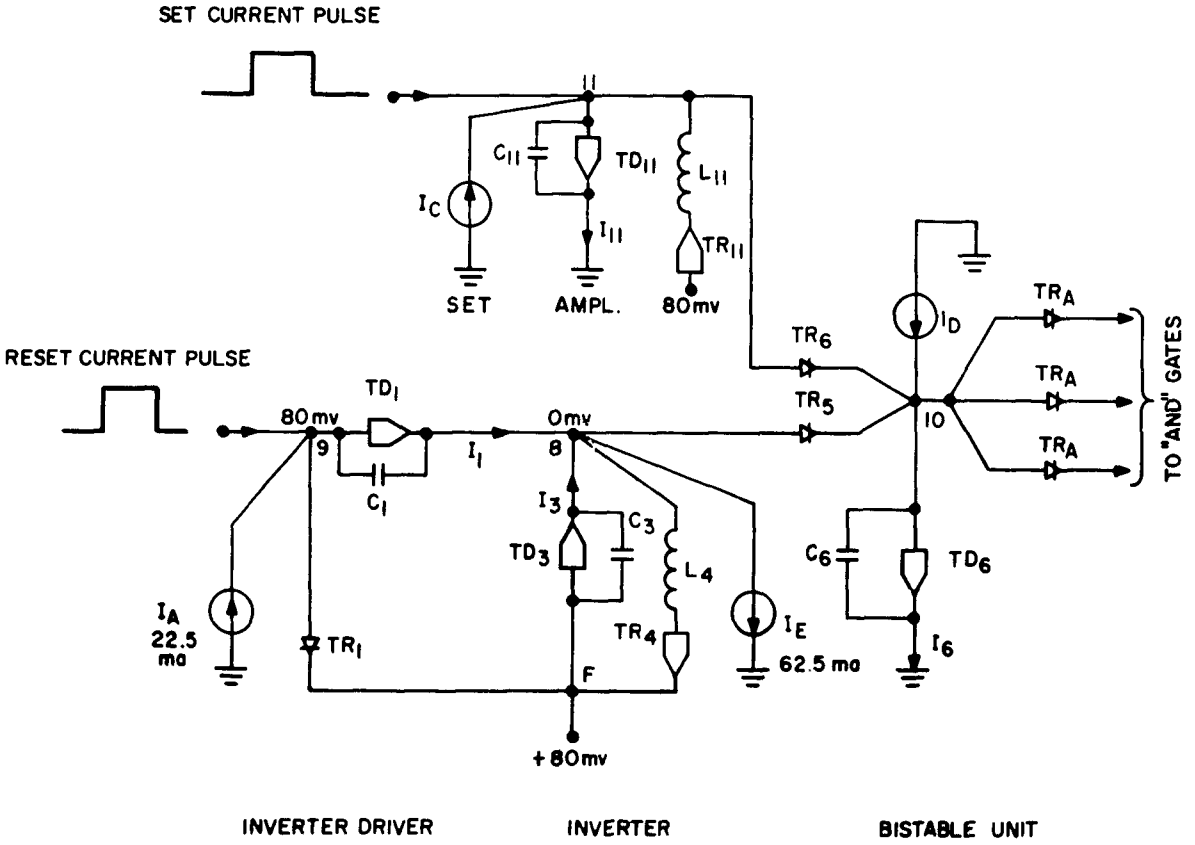


Figure 2-32. Simplified Diagram of Bistable Circuit

a. Setting

The set amplifier consists of a tunnel diode monostable circuit. Since this type of circuit has been described previously, its function here will be mentioned only briefly. Figure 2-33 shows the tunnel diode characteristic of the set amplifier. Superimposed on this characteristic is a load line resulting from the current source (I_C) and the tunnel rectifier (TR_{11}). The two characteristics have one stable intersection designated as "L". When a pulse is applied to the set input, the load line of Figure 2-33 moves up for the duration of the pulse. The circuit becomes temporarily unstable, thus causing it to switch along the trajectory indicated by the dotted lines. This trajectory is a plot of current I_{11} vs. the voltage at node 11 (Figure 2-32). This circuit is designed so that about a 7-ma set input is required to initiate switching. The current of TD_{11} flows through TR_6 into TD_6 of the bistable circuit.

The idealized switching characteristic of the bistable circuit is shown in Figure 2-34. It consists of a tunnel diode intersected by a load line at two stable points, "o" and (1). This load line is formed by the combined characteristic of the three AND gates which TD_6 is driving. Assuming that TD_6 is in the "o" state, the current supplied by the set amplifier causes TD_6 to switch over the peak along the indicated trajectory and stop at point (1) The bistable circuit is thus set to its high state.

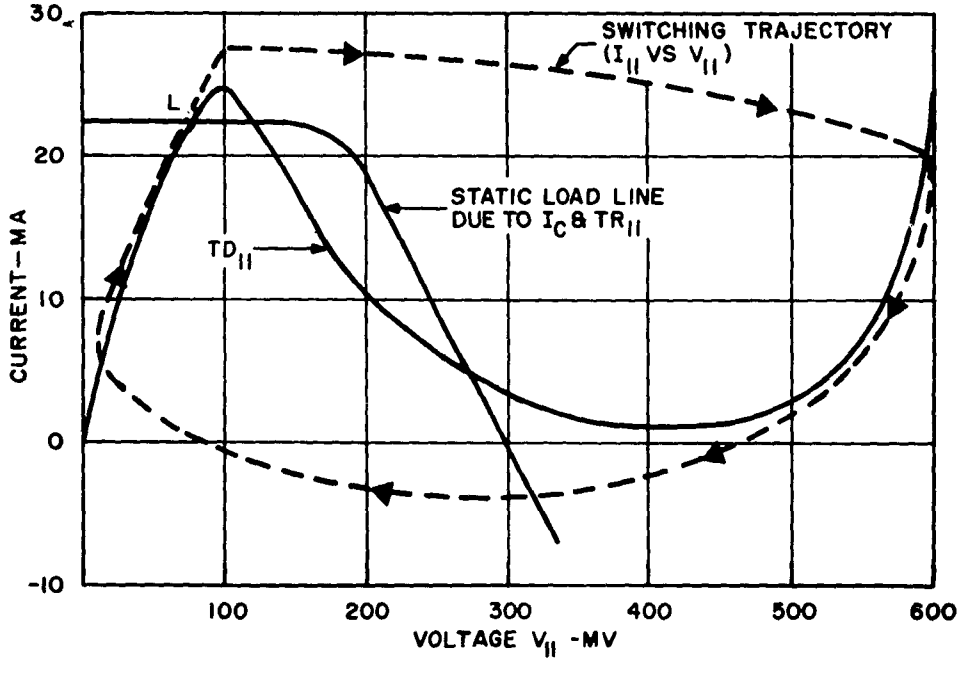


Figure 2-33. Idealized Switching Characteristic of Set Amplifier

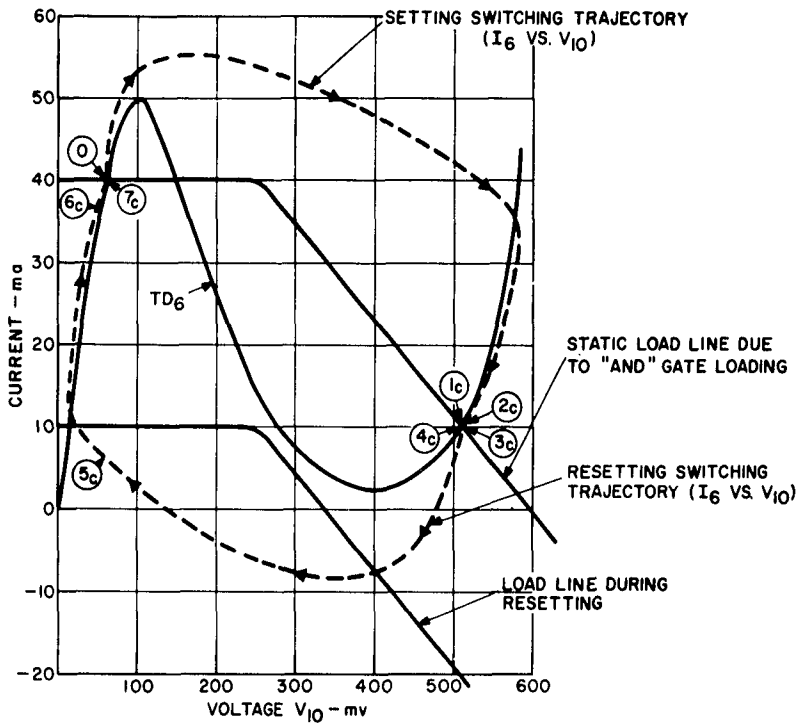


Figure 2-34. Idealized Switching Characteristic of Bistable Circuit

b. Resetting

The operation of the reset circuitry, which consists of the inverter driver and inverter, is more complex and will therefore be described in greater detail. The reset action may be divided into several steps listed in sequence of occurrence. After the application of a reset pulse (Figure 2-32):

(1) The inverter driver switches

(2) The inverter switches

(3) The bistable circuit switches to its low state

(4) All circuits settle down to their original states (except the bistable circuit which remains in the low state). This is referred to as the recovery period.

The idealized switching characteristic of the inverter driver and inverter are shown in Figure 2-35 and Figure 2-36, respectively. Note that the characteristics and the trajectories have been idealized wherever necessary in order to simplify the analysis. Thus at steady state, in Figure 2-32 the currents in TR_1, TR_4, TR_5, TR_6 and TR_{11} are zero. Initially then, $I_1 = I_A = 22.5$ ma, $I_3 = I_E - I_1 = 62.5 - 22.5 = 40$ ma.

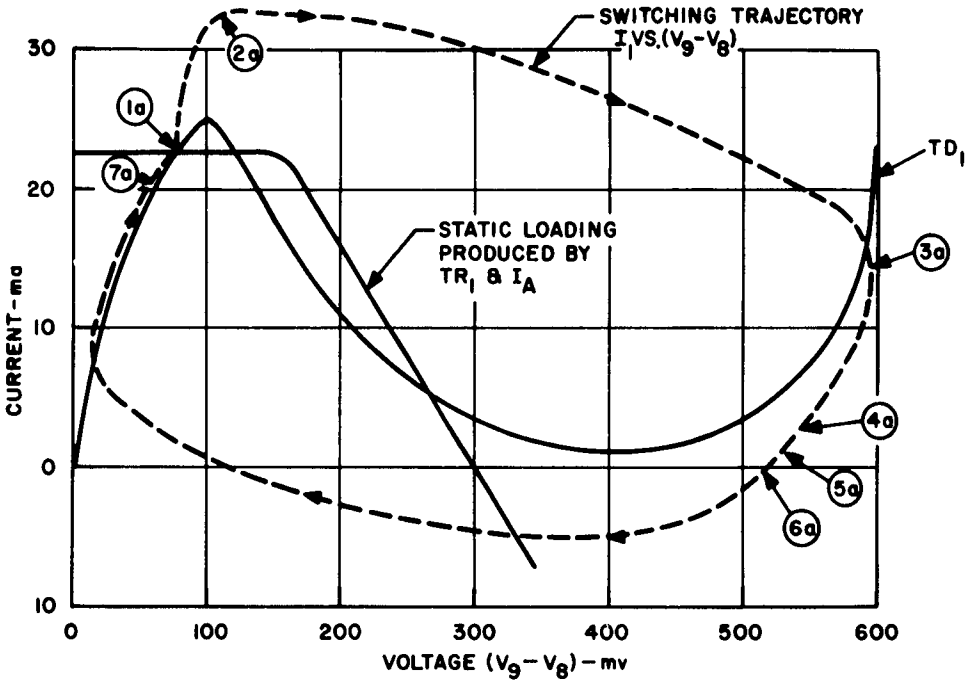


Figure 2-35. Idealized Switching Characteristic of Inverter Driver

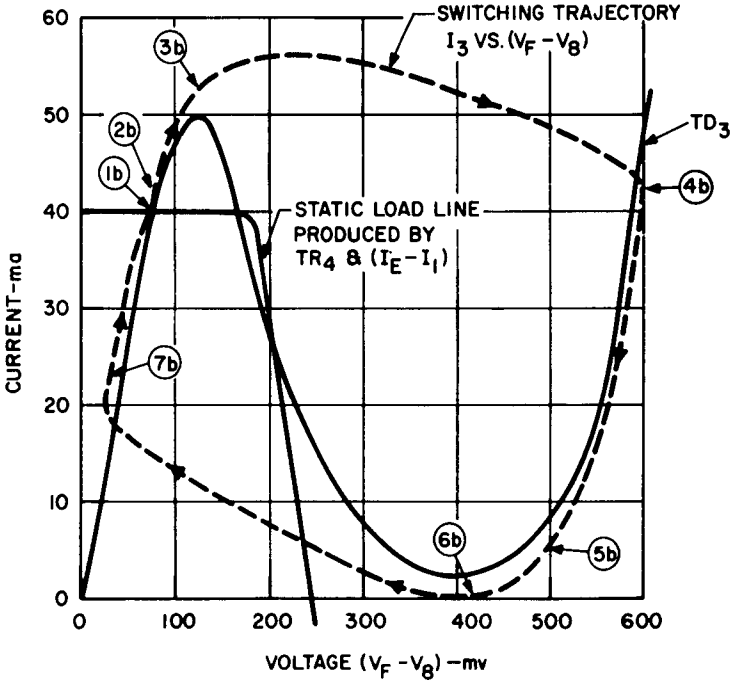


Figure 2-36. Idealized Switching Characteristic of Inverter

When a 10-ma positive current pulse is forced into node 9, the current I_1 increases from 22.5 to 32.5 ma. This current exceeds the peak current of TD_1, causing it to switch from point (1a) to point (3a) along the indicated trajectory of Figure 2-35. Up to this time, the voltage across TD_3 has undergone very little change. This is indicated by point (3b) of Figure 2-36. The corresponding points reached by the bistable unit are shown in Figure 2-34 by the numbers with the c subscripts.

The input has thus caused the voltage at node 1 of Figure 2-32 to increase from 80 mv to about 500 mv. This causes TR_1 to conduct. Since the current into node 1 is constant, conduction of TR_1 causes current I_1 in TD_1 to decrease.

As soon as current I_1 starts decreasing, I_3 starts increasing since $I_3 = I_E - I_1$. (Note TR_4 and TR_6 are not conducting at this time.) I_3 eventually exceeds the peak of TD_3 (point (3b) Figure 3-36) causing TD_3 to switch along the indicated trajectory to point (4b). The voltage across TD_3 ($V_8 - V_F$) is now about -550 mv and the voltage at node 8 is $V_8 = -470$ mv. When TD_6 is high, the voltage at node 10 is approximately 500 mv. The voltage across TR_5 ($V_8 - V_{10}$) now becomes -470-500 = - 970 mv, which is sufficient to cause reverse conduction in TR_5. The idealized characteristic of TR_5 is shown in Figure 2-37.

The flow of current in TR_5 diverts most of the current from the current source, I_D, causing the static load line of Figure 2-34 to move down. When the load line moves down such that the intersection at (1c) becomes unstable or disappears,

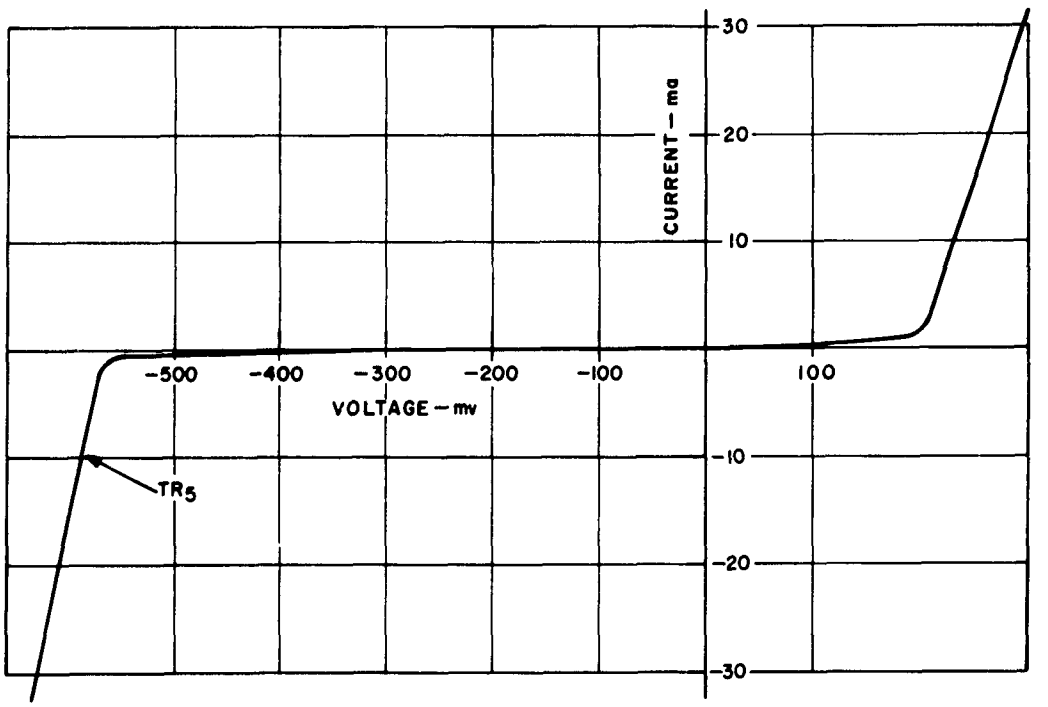


Figure 2-37. Idealized Coupling Rectifier Characteristic for Inverter

TD_6 becomes temporarily unstable and starts switching towards point (6c) along the indicated trajectory. It should be remembered that these are simplified trajectories merely showing the general path of switching. Any deviations not considered essential in describing the basic mode of operation have been omitted. Accurate trajectories will be presented later.

The switching of the bistable unit is complete when it reaches the "0" state. As indicated by their static load lines, the only stable points for the inverter driver and inverter are (1a) and (1b), respectively (Figure 2-35 and Figure 2-36). Consequently, the inverter driver and inverter continue switching along their indicated trajectories until they reach these stable points. This completes the reset action.

2. Transient Analysis Using a Digital Computer

The circuit of Figure 2-32 was simplified for the purpose of explaining its basic mode of operation. In the practical case, however, actual characteristics and stray circuit elements must be considered. A schematic diagram representing the reset action of the actual circuit to a fair degree of accuracy is shown in Figure 2-38. Here, each tunneling device is considered to be shunted by a stray capacitance and in series with a stray inductance. Resistors R_6, R_8 and R_9 are the shunting resistances of the current supply sources. R_0 represents the output resistance of the preceding stage. The combination of TR_7, C_7, and L_7 represents the static and dynamic loading due to the three AND gates. The steady state currents and voltages indicated on the diagram represent nominal operating conditions.

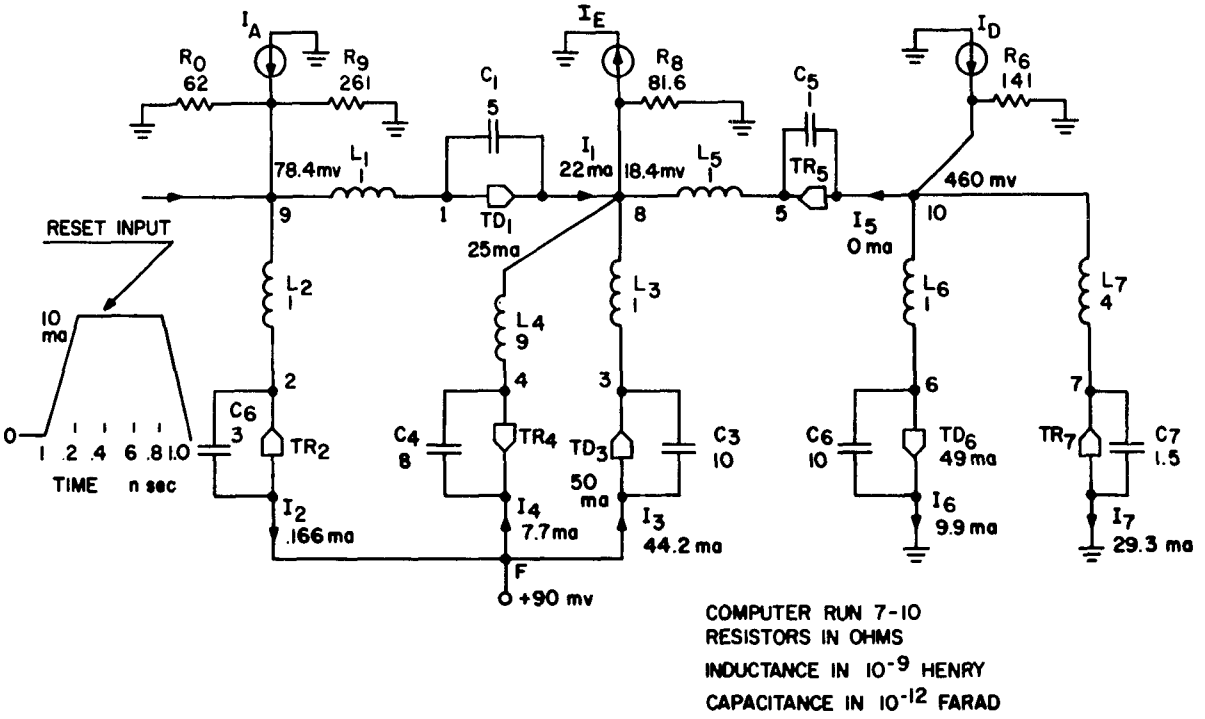


Figure 2-38. Equivalent Circuit used for Analyzing Reset Action of Bistable Circuit on 501 Computer

The differential equations governing the reset behavior of this circuit were solved with the RCA 501 digital computer. These results are presented in Figure 2-39 through Figure 2-48. The computer results, compared with laboratory results, showed good agreement.

3. D-C Tolerance Analysis

The choice of circuit components and voltages was based on considering the following four worst-case conditions:

(a) Setting of Bistable Unit

(b) Resetting of Bistable Unit

(c) Switching of Inverter

(d) Switching of Inverter Driver

Following are the component tolerances considered:

TABLE 2-1
COMPONENT TOLERANCES

Parameter	Symbol	% Variation
Tunnel diode peak current	I_p	±2
Tunnel diode peak voltage	V_c	±5
Tunnel rectifier forward current		±5
6-volt supply voltage	V_a, V_c, V_d, V_e	±2
90-mv supply voltage	V_f, V_g	±10
All resistors		±2

Refer to Figure 2-49 and Figure 2-50 for additional definitions.

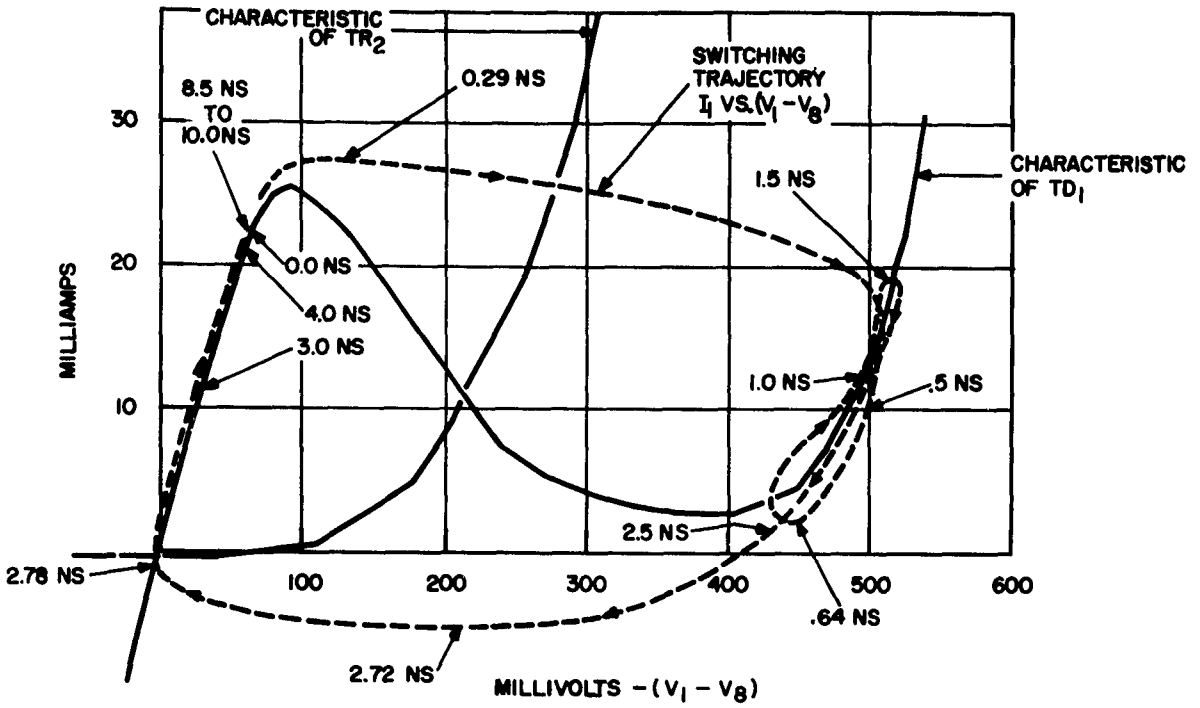


Figure 2-39. Inverter Driver Switching Characteristic Calculated with Digital Computer (Circuit of Figure 2-38)

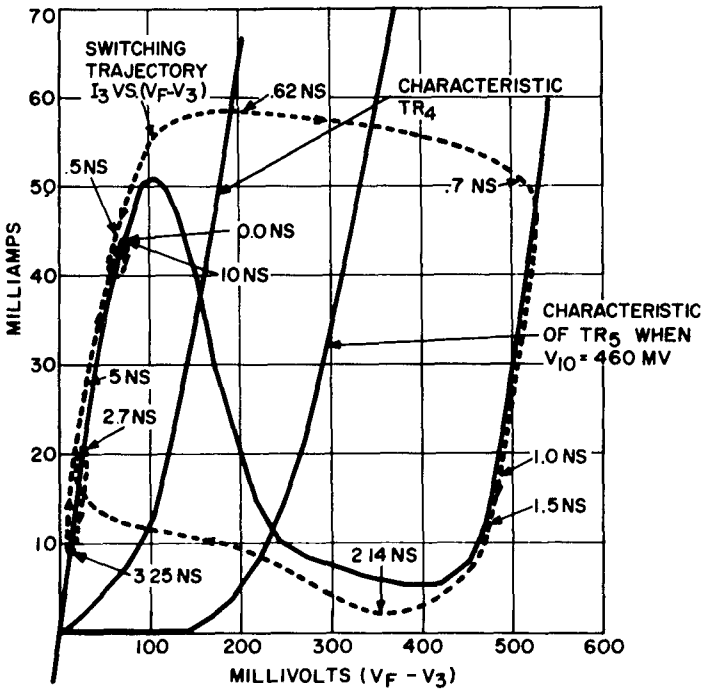


Figure 2-40. Inverter Switching Characteristic Calculated with Digital Computer (Circuit of Figure 2-38)

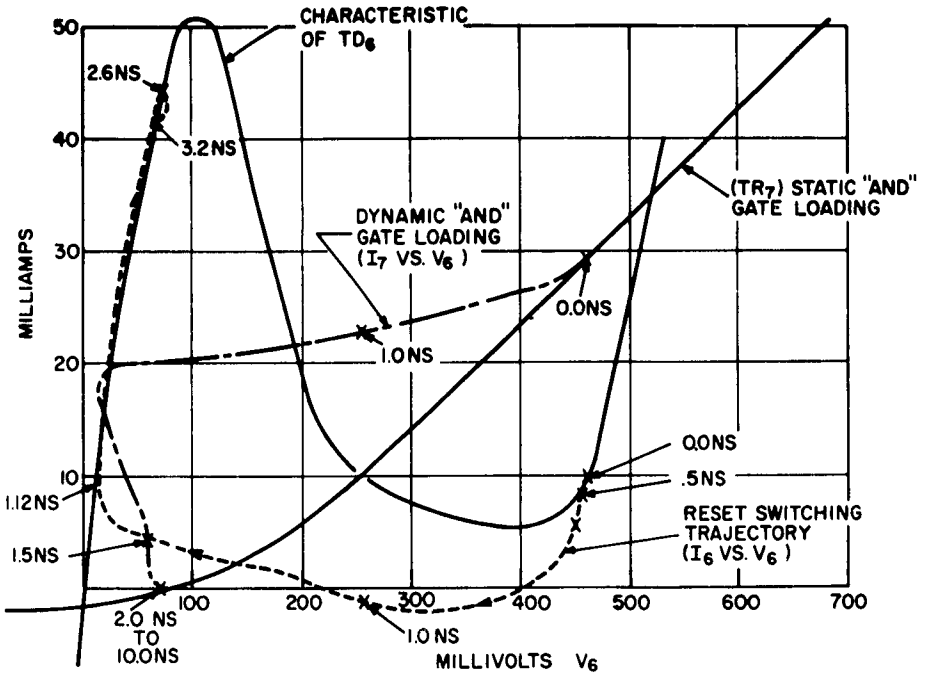


Figure 2-41. Bistable Reset Switching Characteristic Calculated with Digital Computer (Circuit of Figure 2-38)

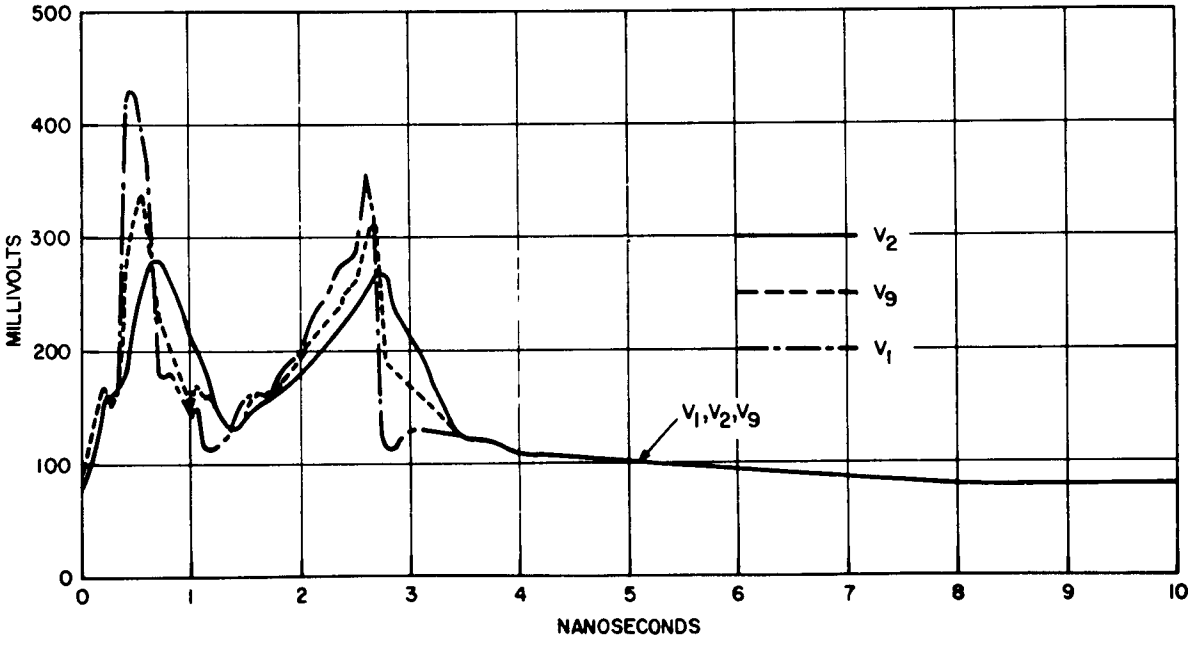


Figure 2-42. Voltage Waveforms of Inverter Driver (Circuit of Figure 2-38)

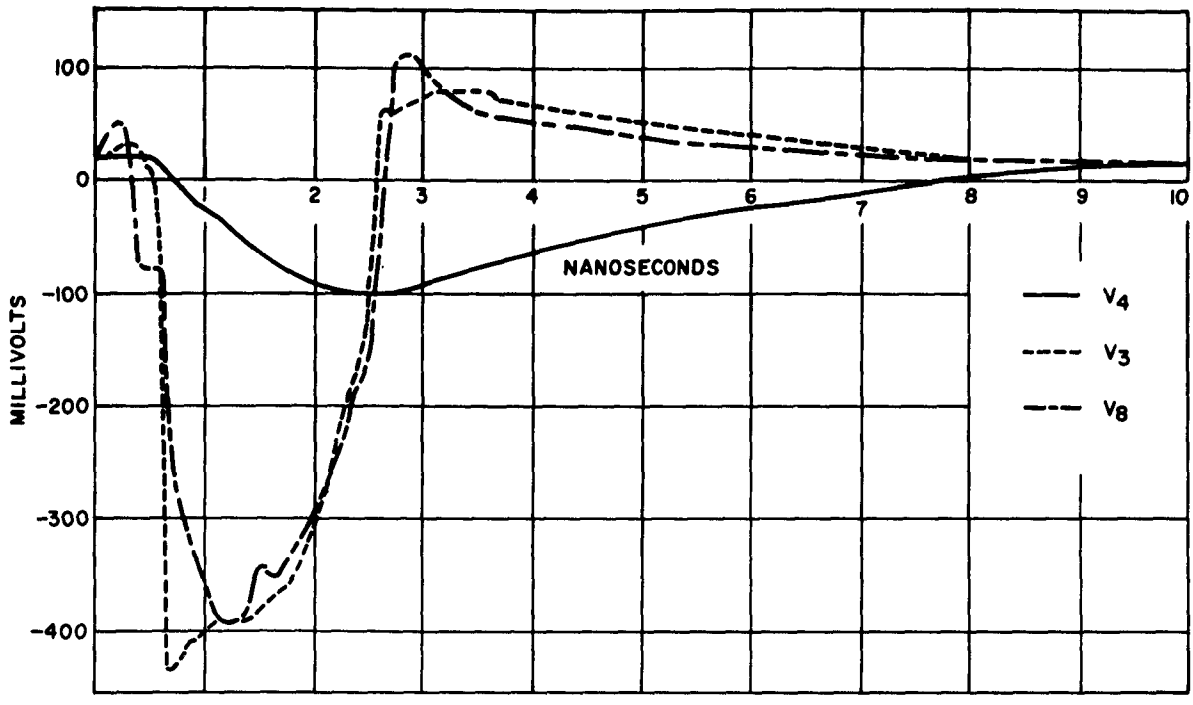


Figure 2-43. Voltage Waveforms of Inverter (Circuit of Figure 2-38)

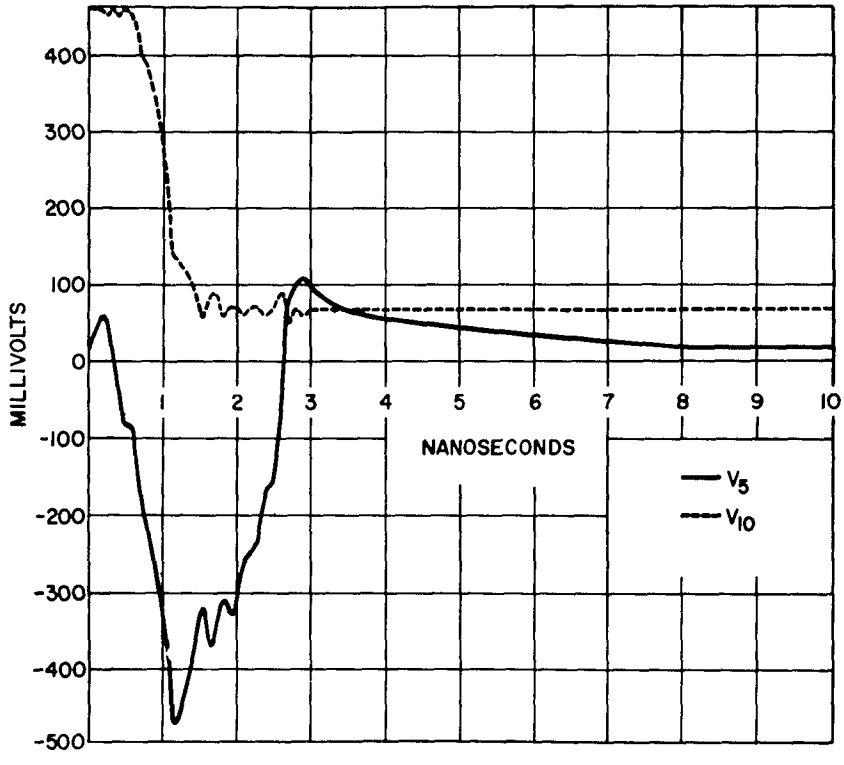


Figure 2-44. Voltage Waveforms of Bistable Diode (Circuit of Figure 2-38)

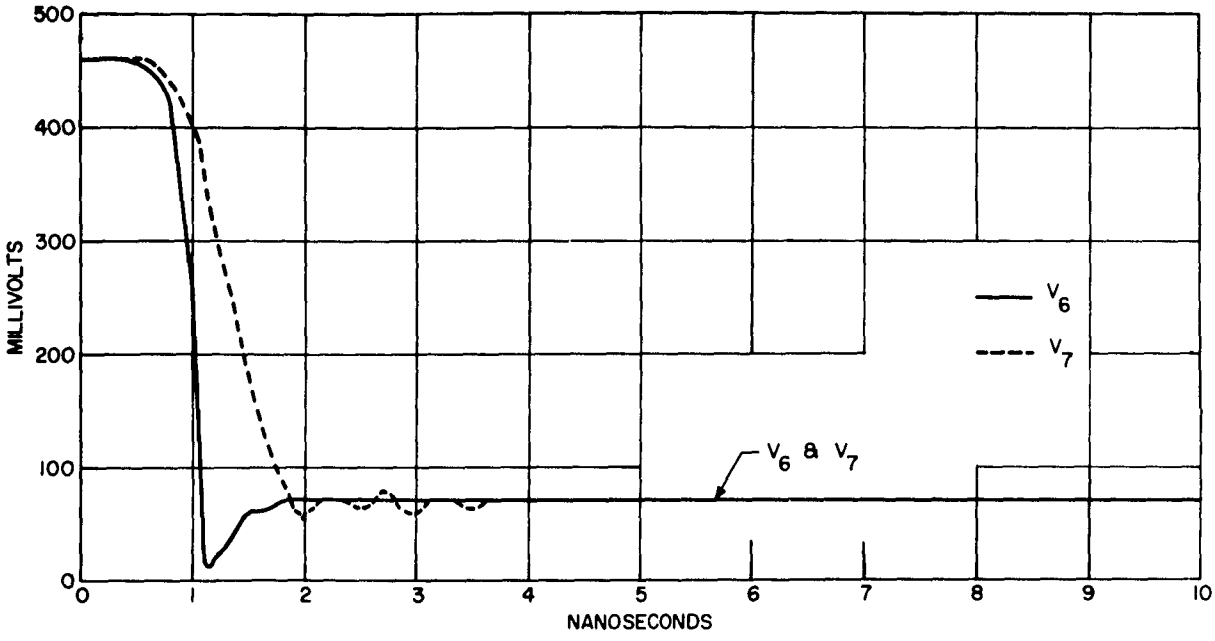


Figure 2-45. Voltage Waveforms of Bistable Diode (Circuit of Figure 2-38)

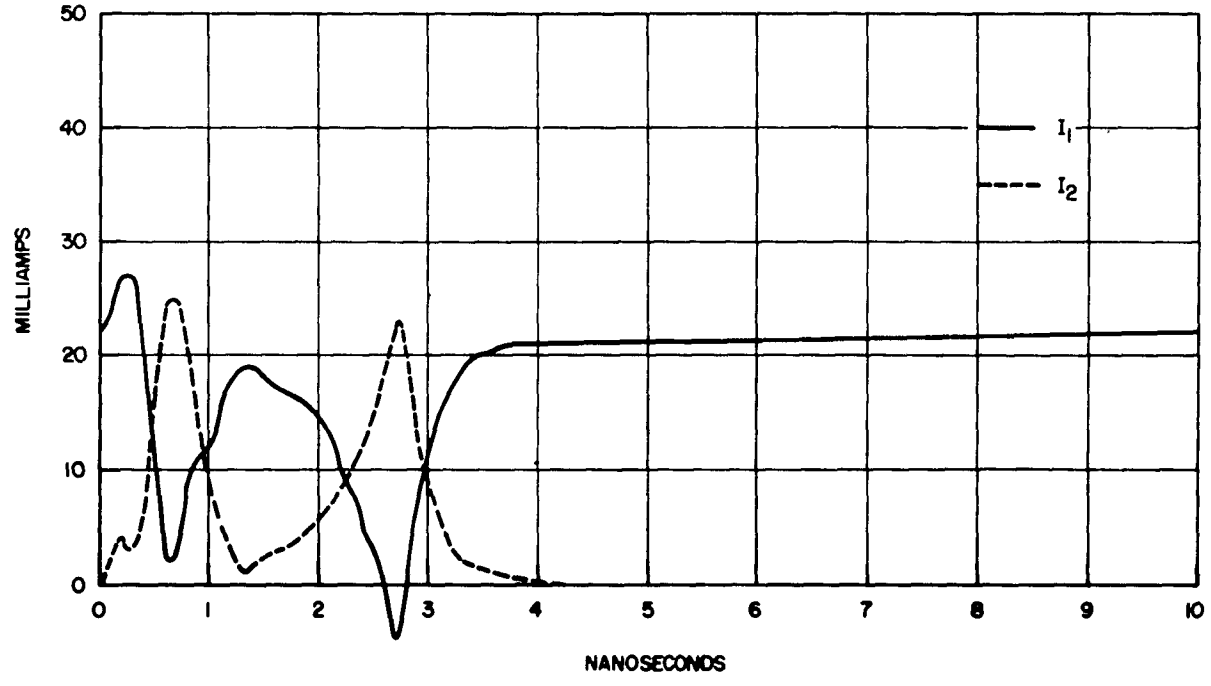


Figure 2-46. Current Waveforms of Inverter Driver (Circuit of Figure 2-38)

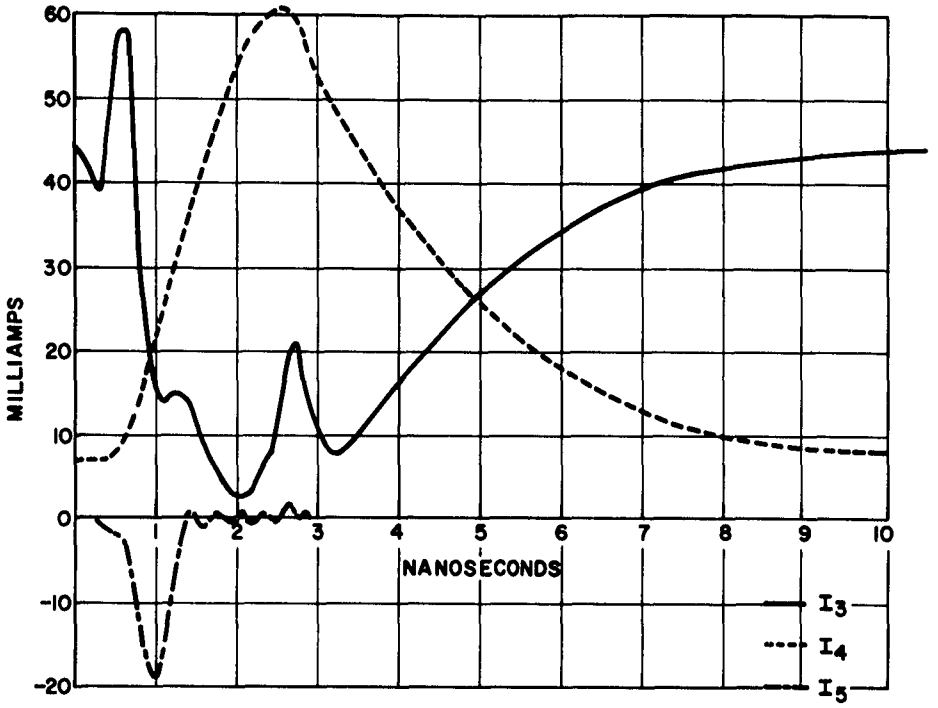


Figure 2-47. Current Waveforms of Inverter (Circuit of Figure 2-38).

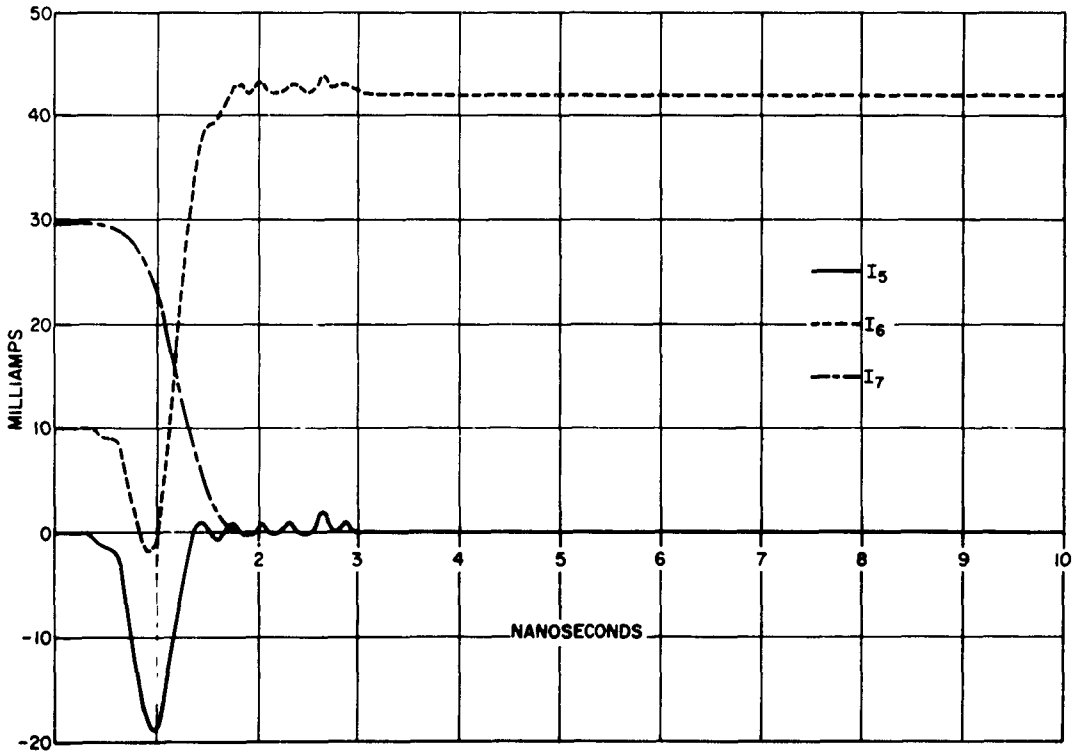


Figure 2-48. Current Waveforms of Bistable Unit (Circuit of Figure 2-38)

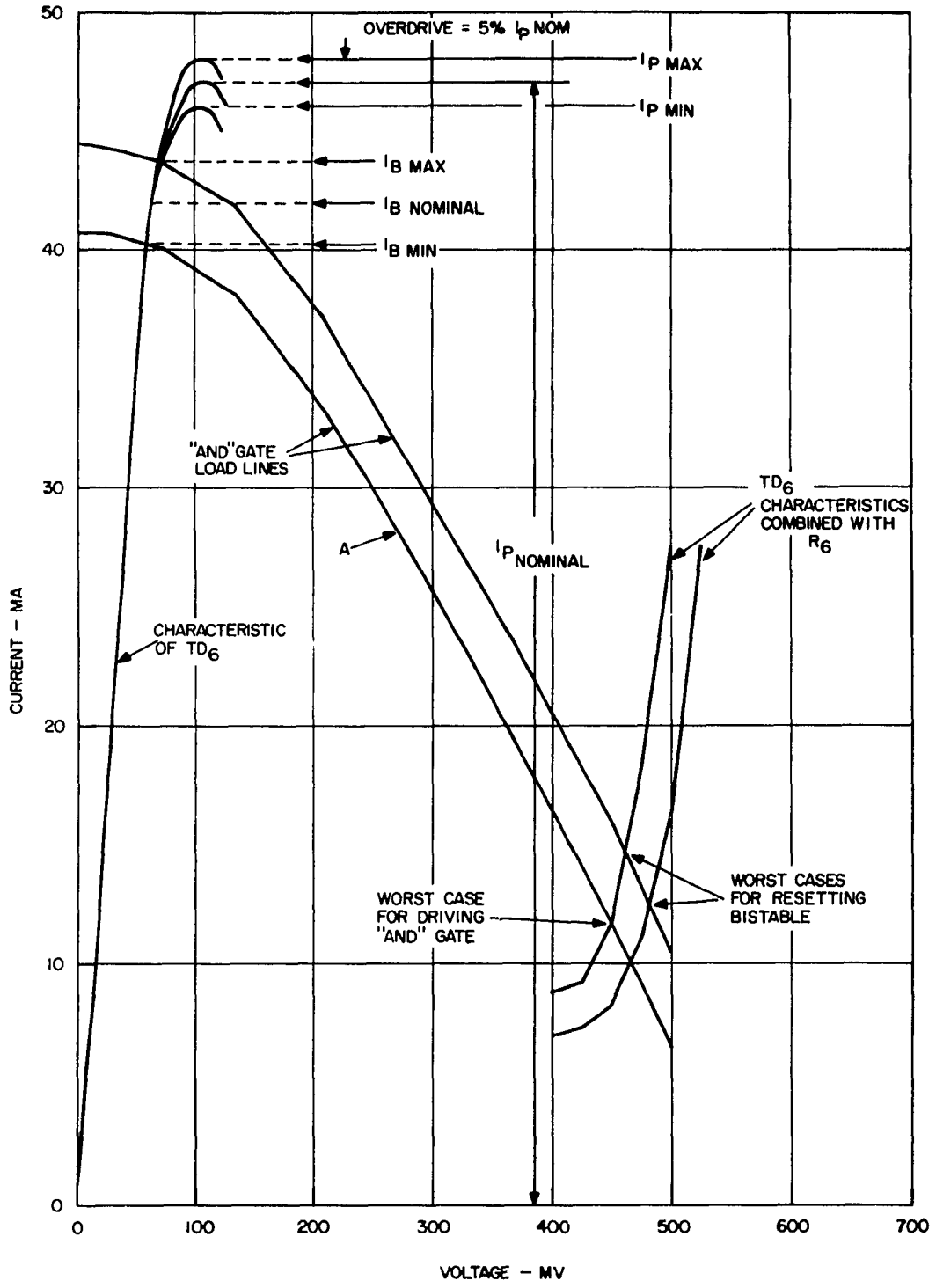


Figure 2-49. Tolerance Analysis of Bistable Diode

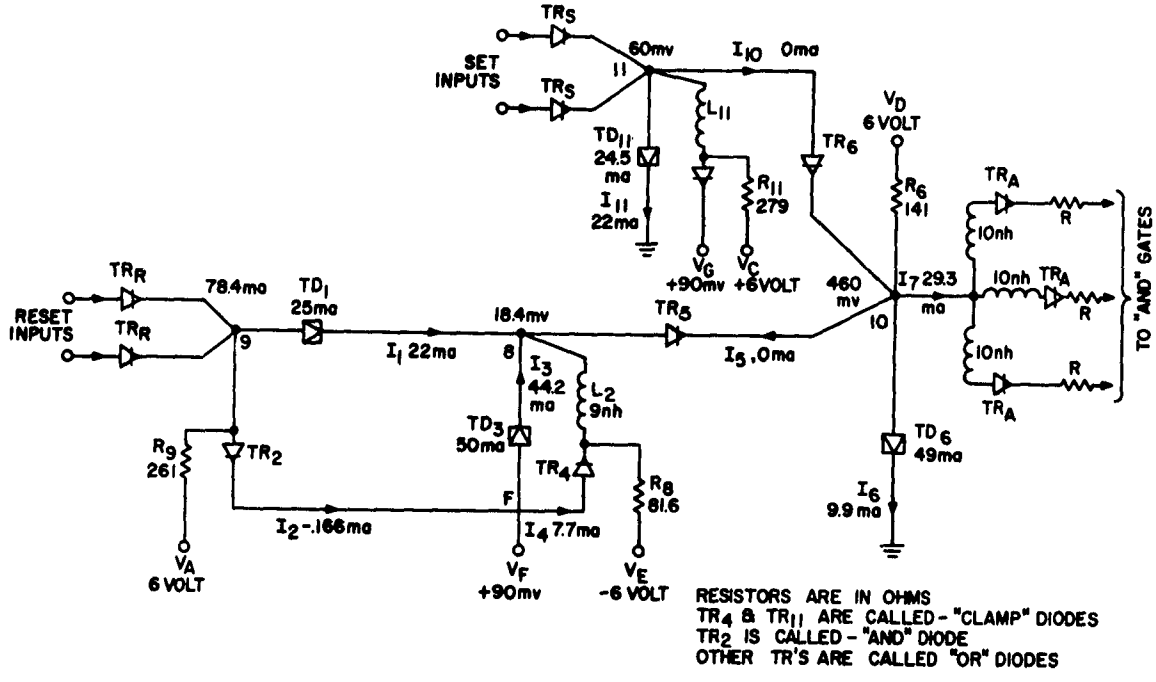


Figure 2-50. Schematic Diagram of Bistable Circuit with Nominal Values

a. Bistable Unit

As pointed out previously, the two stable states of TD_6 (Figure 2-32) are determined by the AND gate loading. The current required for setting or resetting TD_6 is sharply affected by the impedance presented to it by the AND gate. Consequently, in making a tolerance analysis of the bistable unit, the variations in the AND gate input characteristic must be considered. This is illustrated in Figure 2-49, which shows the characteristic of TD_6 with its variations. Superimposed on this characteristic are some of the load lines the AND gate might present. One of the conditions imposed upon TD_6 by the AND gate is that when the combined input to the three AND gates presents a load line designated by curve A in Figure 2-49, the minimum bistable output must be 450 mv. This assures that the minimum level in any AND gate will not be less than 7.8 ma. The point at which curve A intersects TD_6 in the low voltage region gives $I_{B\ min} = 40.2$ ma (this is the minimum current that may flow in TD_6 when it is in the low voltage state). If I_B is assumed to vary ±4% due to variations in supply voltage (V_D) and source resistance (R_6) of Figure 2-50, then

$$I_{B\ min} = I_B - .04\, I_B \tag{1}$$

or

$$I_B = \underline{42.0\ ma} \tag{2}$$

and

$$R_6 = \frac{V_D - V_{10}}{I_B} = \frac{6000 - 70}{42} = \underline{141 \text{ ohm}} \tag{3}$$

where V_{10} is the voltage at node 10 when TD_6 is in the low voltage state (Figure 2-50).

The choice of TD_6 is based on two considerations: (a) the peak current of TD_6 should be as small as possible to allow the use of a smaller set input and (b) the peak current must be large enough to prevent TD_6 from switching without an input. In order to satisfy (b), the following relationship must be satisfied:

$$I_{p\ min} \geq I_{B\ max} + 0.5\ I_p \tag{4}$$

The last term in Eq. 4 is a safety margin. The variation in I_p is assumed to be ±2%, consequently, Eq. 4 becomes:

$$.98\ I_p = 1.04\ I_B + .05\ I_p \tag{5}$$

or

$$I_p = \underline{47 \text{ ma}}$$

The minimum set input is made large enough to provide an overdrive of $.05\ I_p$ under worst-case conditions. This may be expressed as:

$$I_{set\ min} \geq I_{p\ max} + .05\ I_p - I_{B\ min} \tag{6}$$

$$= 1.02\ I_p + .05\ I_p - .96\ I_B$$

$$I_{set\ min} = \underline{10 \text{ ma}}$$

These values are indicated in Figure 2-49. The output available from the set amplifier was calculated to be 16 ma minimum. Since the set requirements were less than that available from the set amplifier, the peak current of TD_6 was raised to 49 ma. This permits the use of a more readily available tunnel diode for the bistable circuit.

TD_6 is most difficult to reset when maximum current is flowing through it. The two points which represent worst cases for resetting are indicated in Figure 2-49. The diode currents corresponding to these points are lower by about 3.5 ma. This is due to the fact that in the construction of Figure 2-49, a combined characteristic of TD_6 and R_6 was used.

b. Inverter and Inverter Driver

Experiments and computations have indicated that in order to reset the bistable circuit, a 50-ma peak current tunnel diode will be required for the inverter. This dictated the choice of a 25-ma peak current tunnel diode for the inverter driver. Tolerance analyses, similar to those shown for TD_6 in Figure 2-49, were carried out for the inverter and inverter driver.

The results and the assumptions made to set up these worst-case conditions are described below.

The worst case for switching the inverter occurs when:

(Refer to Figure 2-32 and Table 2-1 for definition of symbols)

I_{p3} is maximum = 51.0 ma

V_{p3} is maximum = 105.0 mv

V_E is maximum = 5.88 volts

R_8 is maximum = 83.23 ohms

V_A is maximum = 6.12 volts

R_9 is minimum = 255.8 ohms

V_F is minimum = 81 mv

V_{10} is maximum = 532 mv

TR_4 is conducting maximum

TR_5 is conducting maximum

The significant node voltages and currents under these conditions are:

V_9 = 85 mv

V_8 = 16.8 mv

I_1 = 23.5 ma

I_3 = 40.8 ma

I_2 = .075 ma

I_4 = 6.2 ma

I_5 = 1.5 ma

The worst case for switching the inverter driver occurs when:

I_{p1}	is max = 25.5 ma	V_E	is min = 5.88 volts
V_{p1}	is max = 105 mv	R_8	is max = 83.23 ohms
V_A	is min = 5.88 volts	V_F	is max = 99 mv
R_9	is max = 266.2 ohms	TR_2	is conducting maximum
I_{p3}	is max = 51.0 ma	TR_4	is conducting maximum
V_{p3}	is min = 95.0 mv		

The significant node voltages and currents under these conditions are:

V_9	= 101.4 mv	I_3	= 43.5 ma
V_8	= 36.1 mv	I_4	= 6.3 ma
I_1	= 21.8 ma		
I_2	= .02 ma		

4. Experimental Circuit

The complete bistable circuit is shown in Figure 2-50. The extreme voltage and current variations under which this circuit may be expected to operate are listed below. These variations were obtained by considering all possible variations in circuit elements and supply voltages.

V_9	50 mv	to	122 mv
V_8	- 13 mv	to	46 mv
V_{10}	445 mv	to	495 mv
V_{11}	57 mv	to	77 mv
I_1	22.1 ma	to	23.9 ma
I_3	40.8 ma	to	48.1 ma

The choice of circuit components and design was based on the d-c tolerance calculations and the digital computer results.

The set and reset inputs are applied through tunnel rectifiers to isolate the circuit from preceding logic stages.

The current sources are connected directly to the rectifiers, TR_4 and TR_{11}, instead of to nodes 8 and 11 as shown in Figure 2-32. The difference between the two is very slight. However, the connection in Figure 2-50 is more desirable since it prevents R_8 and R_{11} from loading the tunnel diodes.

The inductances in series with the output rectifiers of TD_6 are used to obtain more efficient reset action. This is due to the fact that during the initial period of resetting, the series inductances prevent the currents in the AND gates from changing and thus permitting more of the reset current to go through TD_6. The addition of inductance, however, increases the time required for establishing a new level in the AND gate, reducing somewhat the overall repetition rate.

The bistable circuit of Figure 2-50 exhibits the following performance.

2 set inputs of 7 ma (minimum) each

2 reset inputs of 8 ma (minimum) each

3 outputs of 10 ma (nominal) each

*Electrical delay:		
Set	3 ns	these are approximate nominal values
Reset	3 ns	
**Delay between:		
Set - Reset	3 ns	
Reset - Set	3 ns	
Reset - Set - Reset	8 ns	
Set - Reset - Set	6 ns	

---

* Delay from the time the input has risen to the time the new level in the AND gate is established.

** Delay from the time the input has risen to the time the new input may be applied.

5. Conclusion

By studying the dynamic and static behavior of the circuit, certain conclusions can be drawn regarding the choice of circuit elements for reliable and optimum performance.

Refer to Figure 2-38.

(a) The inductance L_1, L_2 and L_3 should be kept as small as possible to permit a rapid increase in I_3 during switching of TD_3. This is desirable to prevent loss of switching current into TR_4 and TR_5.

(b) The ratio of L_9 to L_5 must be large enough so that sufficient current can flow through L_5 to permit resetting of TD_6.

(c) L_9 must be large enough so that the inverter recovers after the inverter driver recovers. If the inverter recovers first and the current available for TD_3exceeds the peak of TD_3, the inverter may switch again.

(d) The stray capacitance C_5 across TR_5 should be as small as possible to prevent the bistable from being set with the trailing edge of the inverter pulse.

(e) It will be noticed that the entire inverter is lifted off ground by a bias voltage of 90 mv. Two considerations made this necessary. 1) It is desirable that TR_5 not conduct during steady state. If TR_5 is allowed to conduct, it imposes severe tolerance problems in the inverter. However, with the characteristics available for TR_5 it starts conducting in the reverse direction when there is 450 mv across it. When TD_6 is in the high state, the voltage at node 10 may be as high as 495 mv. Consequently, in order to keep TR_5 from conducting in excess of 2 ma, the voltage across it must be reduced. This is accomplished by raising the voltage at node F, thus reducing the voltage across TR_5. 2) It is desirable that the voltage at node 9 be about 70 mv, which is the approximate voltage at the input of all the other logic gates. However, since TD_1 and TD_3 are connected back-to-back, this voltage would be about zero if point F was grounded. Lifting TD_3 above ground raises the voltage at node 9 to the required value.

(f) It will also be noticed that TR_4, which is acting as a clamp for TD_3, is returned to the same voltage as TD_3. Normally, this is not done since it causes the clamp to conduct at steady state making it harder for TD_3 to switch. This, however, was necessary to prevent the inverter from becoming bistable and never returning to its low state quiescent condition. If a clamp with a sharp enough break was available, this measure would not be necessary.

E. DELAY CIRCIUT

A delay element in the range of 10 to 20 nanoseconds is required in conjunction with the logic circuits to be used in the subsystem. One method of producing delay is through the use of an active delay circuit which also may provide gain. One such delay circuit which was designed and tested is shown in Figure 2-51. This circuit is similar to the bistable circuit previously described in this report and is contained on the same type of wafer. The circuit has two OR inputs and produces a fan-out of two. The output is a pulse of approximately 1 to 2 nanoseconds width, delayed by a fixed amount from the application of an input pulse from a monostable gate. The magnitude of the delay is controlled by adjusting the size of L_1. The circuit uses the inverter of the bistable circuit as its main component. The input pulse triggers the monostable inverter producing a negative pulse whose width is controlled by the size of inductor L_1. The negative pulse is differentiated and the trailing edge of the inverted pulse used to trigger a monostable amplifier. The active circuit method of producing delays has the advantage of providing gain and pulse reshaping along with the delay. Its disadvantage is the tolerance associated with the delay which is a function of the properties of the active elements used. Figure 2-52 shows the waveforms obtained from the delay wafer. The designations of these waveforms are given in Figure 2-51.

F. REPRESENTATION OF TRANSMISSION LINES FOR DIGITAL COMPUTER NUMERICAL INTEGRATION TECHNIQUES

Consider the transmission line shown in Figure 2-53 to be connected in a network that may contain non-linear elements. If the line is ideal, it can be represented as shown in Figure 2-54. The value of $\frac{de_a}{dT}$ that is used in the equivalent circuit is obtained as follows:

Since the voltage on the line is

$$e_{line} = e_{up} + e_{down}$$

and the current in the line is

$$i_{line} = \frac{e_{down} - e_{up}}{R_o}$$

$$e_a = e_{line} - R_o\, i_{line}$$

$$= e_{up} + e_{down} - (e_{down} - e_{up}) = Z_{e\ up}$$

and

$$\frac{de_a}{dT} = Z\,\frac{de_{up}}{dT} \quad .$$

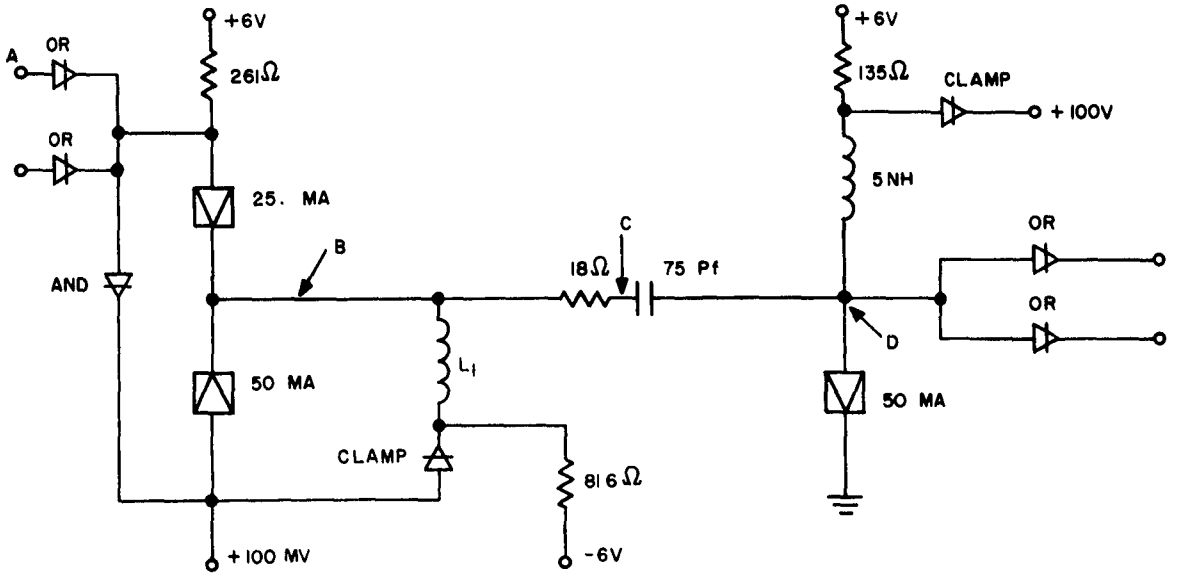


Figure 2-51. Delay Circuit

Figure 2-52. Delay Circuit Waveforms

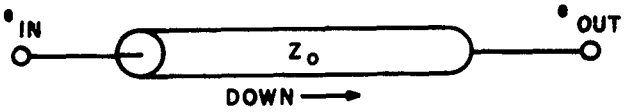


Figure 2-53. Ideal Transmission Line

Figure 2-54. Ideal Line Equivalent

Two tables are constructed in the high-speed memory of the computer and are called the "up table" and the "down table" as shown in Figure 2-55. The number of entries in each table is equal to the time delay of the line divided by the interval of integration used in the numerical analysis. Since the line is initially at rest, both tables contain all zero entries at the start of the problem. The derivatives $\frac{de_{in}}{dT}$ and $\frac{de_{out}}{dT}$ are obtained using values of $\frac{de_a}{dT}$ and $\frac{de_b}{dT}$ from the table and the states of the external circuits at the ends of the line. The derivatives of the reflected waves on the line are obtained as shown in equations 1 and 2.

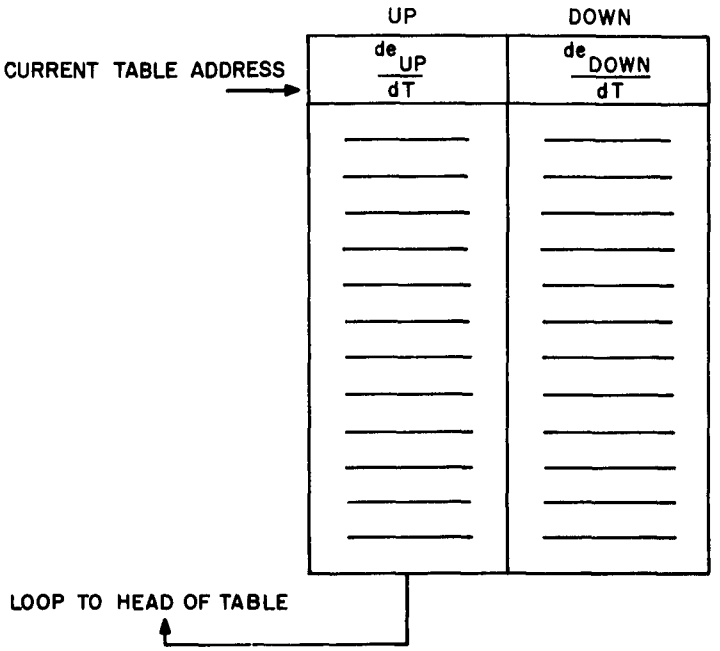


Figure 2-55. Memory Tables for Transmission Lines

$$\frac{de_{down}}{dT_{(reflection)}} = \frac{de_{in}}{dT} - \frac{de_{up}}{dT} \qquad (1)$$

$$\frac{de_{up}}{dT_{(reflection)}} = \frac{de_{out}}{dT} - \frac{de_{down}}{dT} \qquad (2)$$

The result obtained from (1) is placed in the down table at the current address and that from (2) in the up table. The current table address is then incremented by one and the whole process repeated as a subroutine of the main program for the circuit for the next interval of integration. Addressing must be done completely around the table to obtain as an output what was put in one line delay previously. If the line has a constant attenuation for all frequencies, the result of (1) and (2) must be multiplied by a factor less than unity to handle the situation.

Several different programs were written for circuits containing transmission lines; the results agreed very well with that predicted by circuit theory. The waveforms for one of the circuits are included. The circuit, shown in Figure 2-56, consisted of a 35-ma peak current monostable stage driving two 25-ma peak current monostable stages in parallel, through transmission lines with time delays of one nanosecond each. Current and voltage waveforms for this circuit are shown in Figures 2-57 through 2-66. The tunnel diode and rectifier characteristics are shown in Figures 2-67 through 2-71.

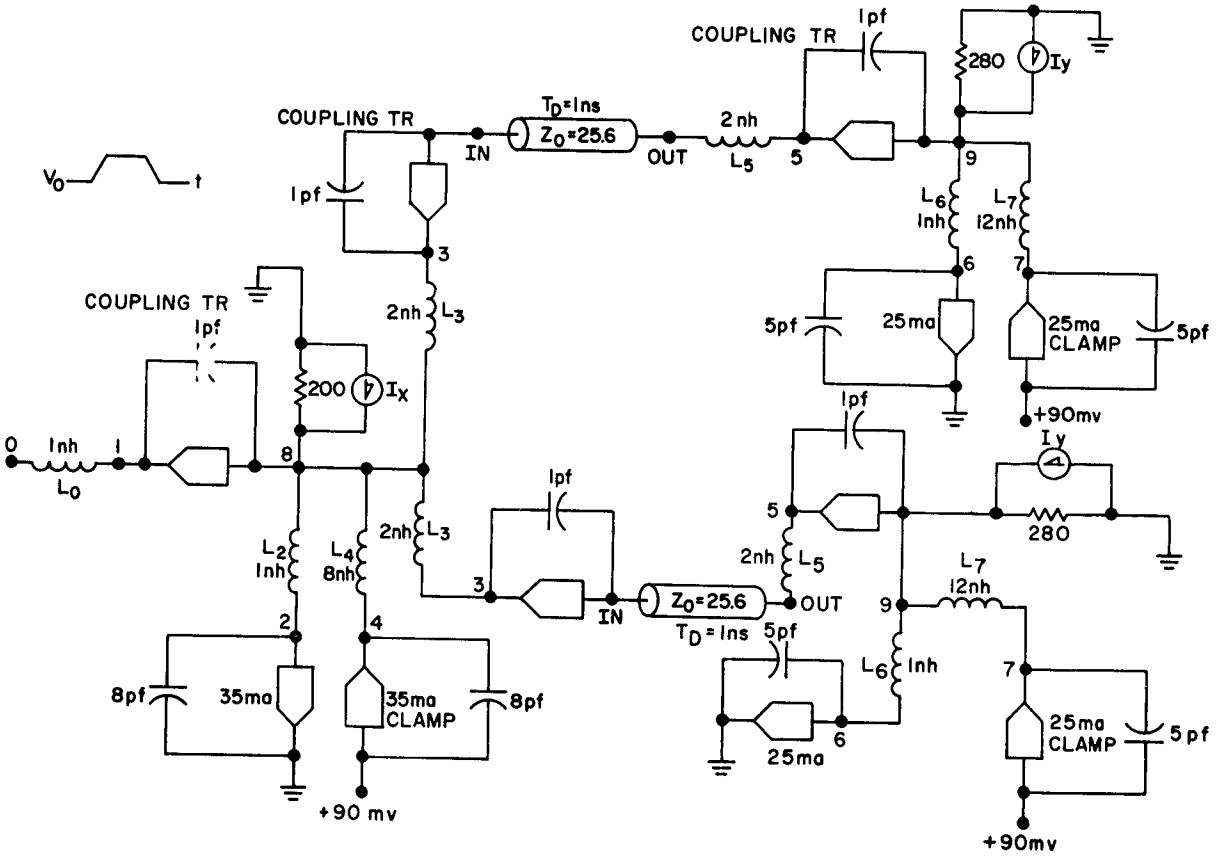


Figure 2-56. Test Circuit

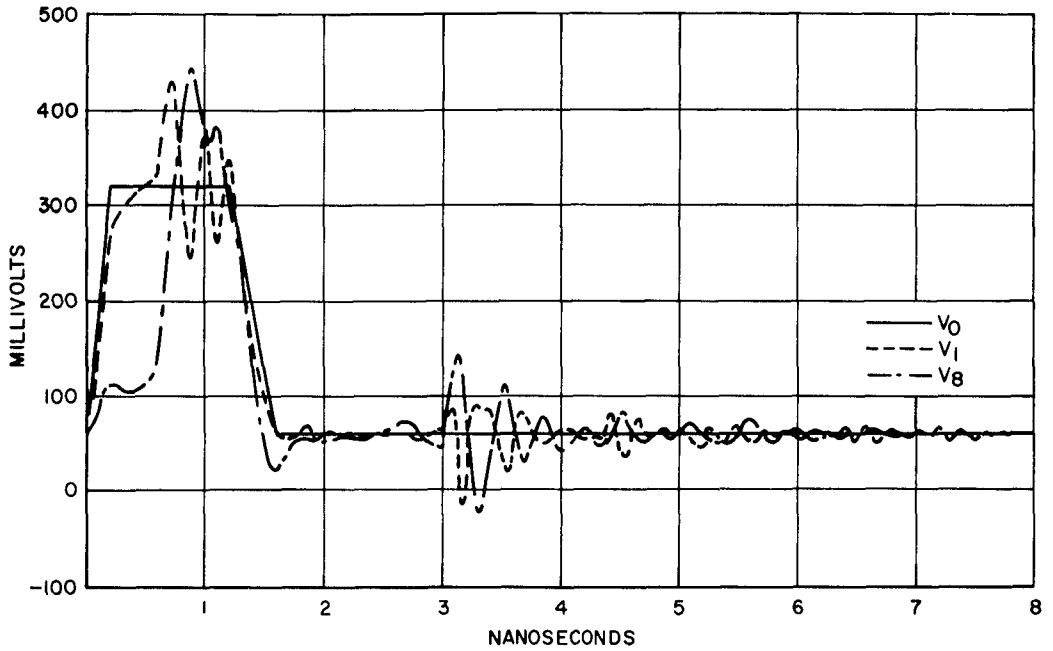


Figure 2-57. Test Circuit Voltage Waveforms

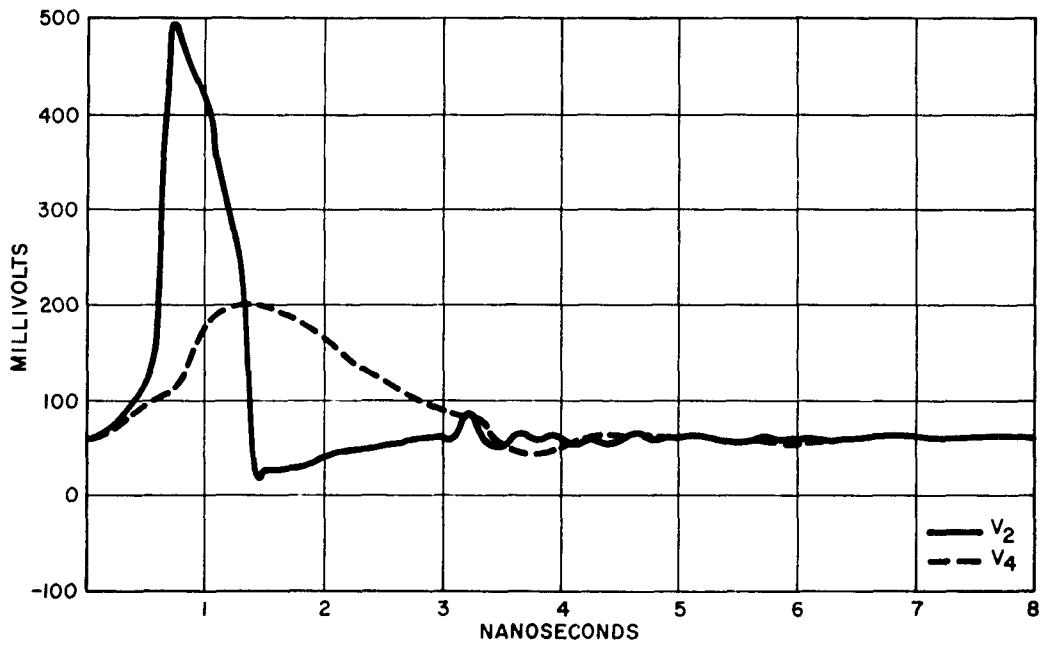


Figure 2-58. Test Circuit Voltage Waveforms

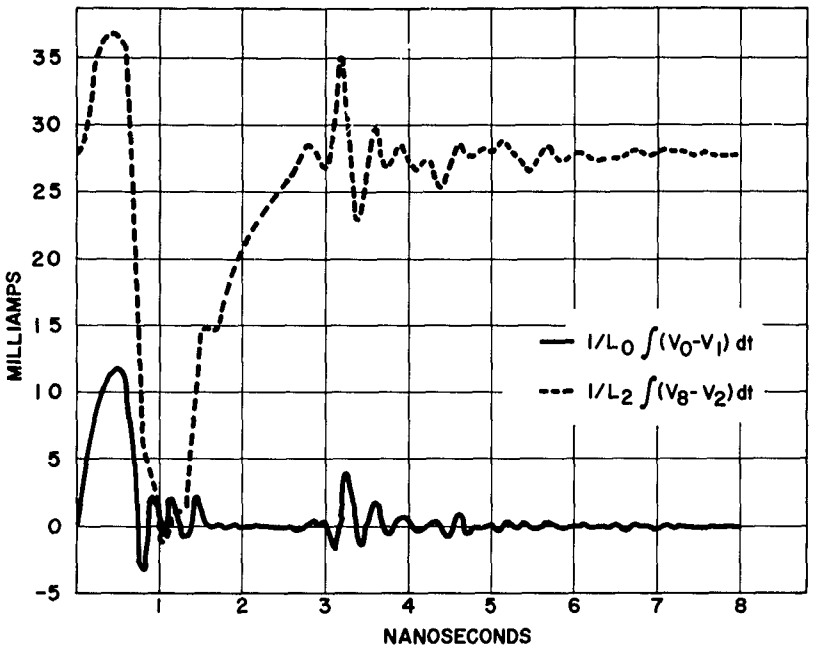


Figure 2-59. Test Circuit Current Waveforms

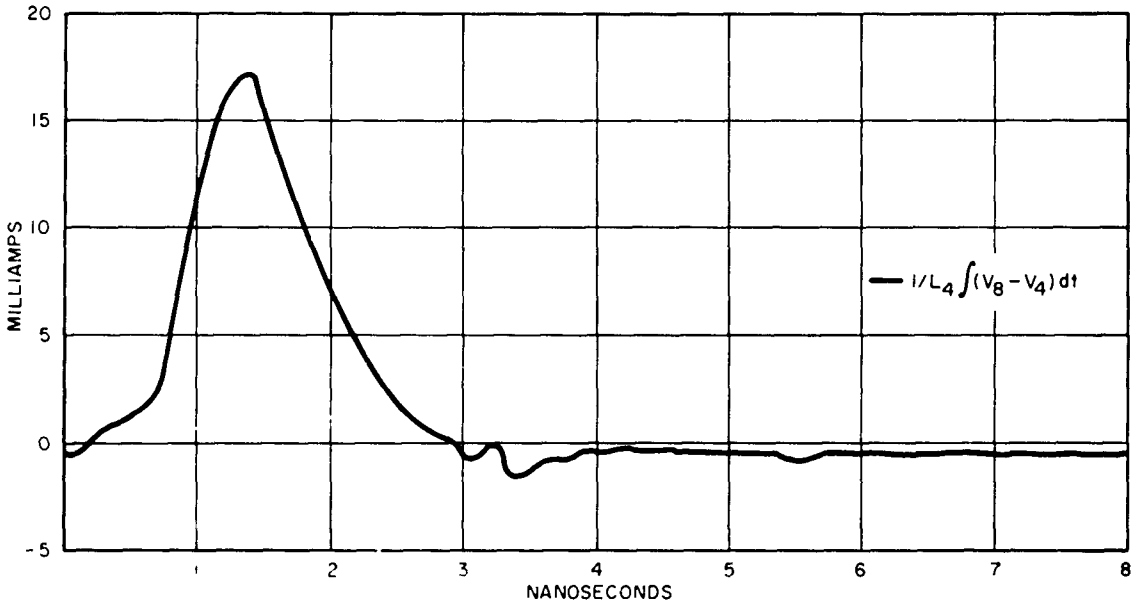


Figure 2-60. Test Circuit Current Waveforms

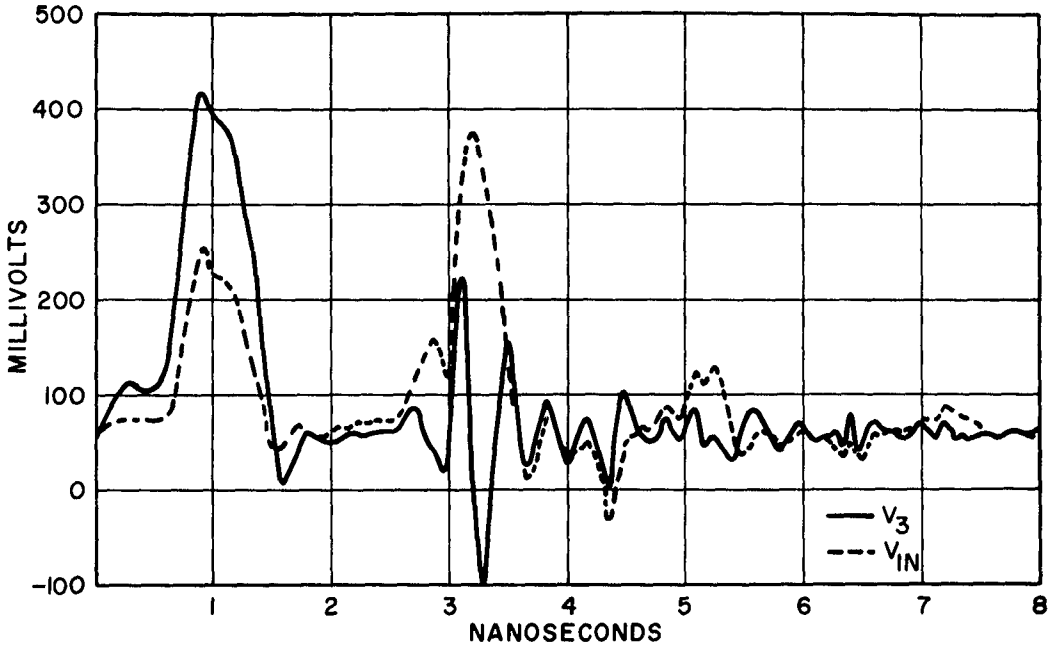


Figure 2-61. Test Circuit Voltage Waveforms

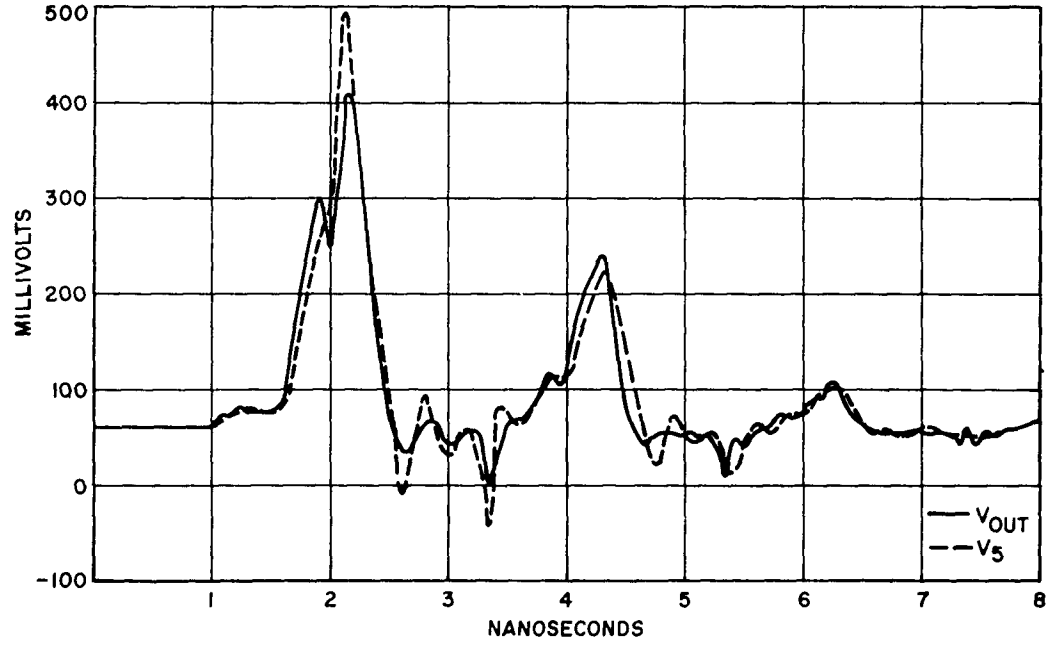


Figure 2-62. Test Circuit Voltage Waveforms

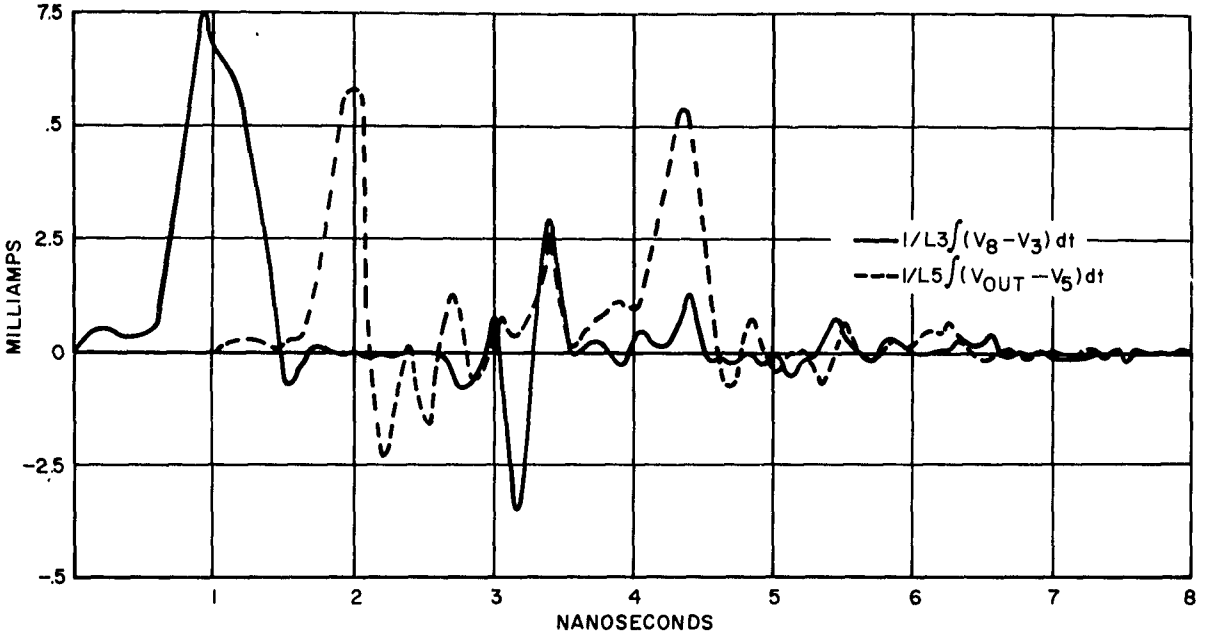


Figure 2-63. Test Circuit Current Waveforms

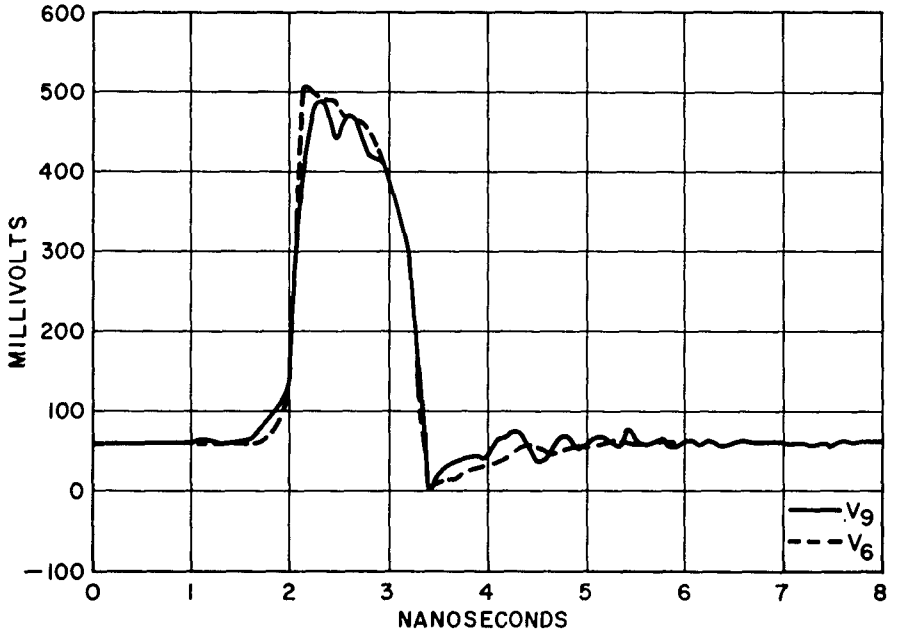


Figure 2-64. Test Circuit Voltage Waveforms

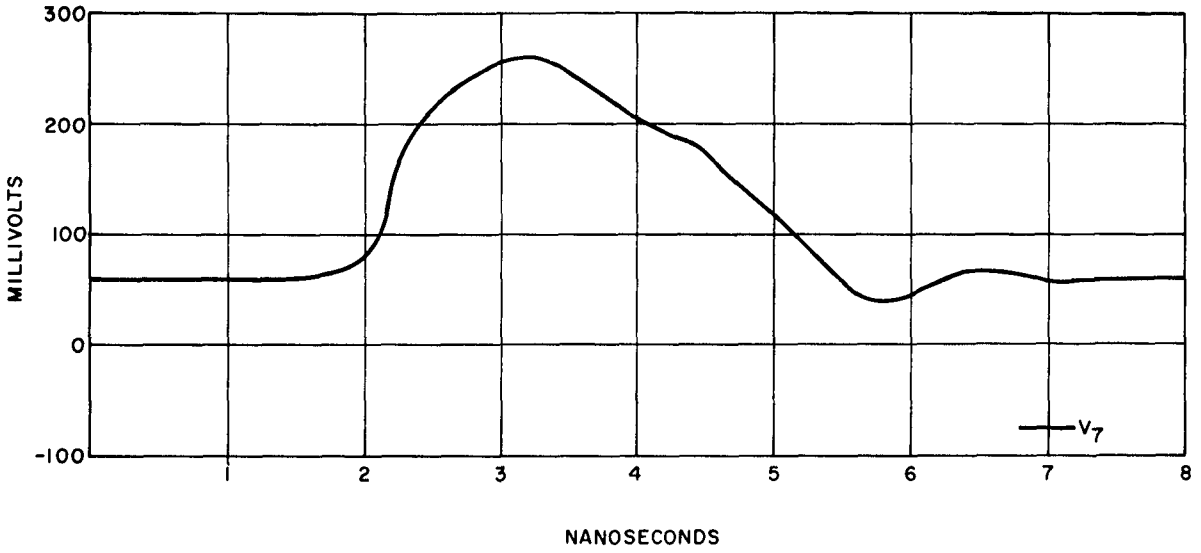


Figure 2-65. Test Circuit Voltage Waveforms

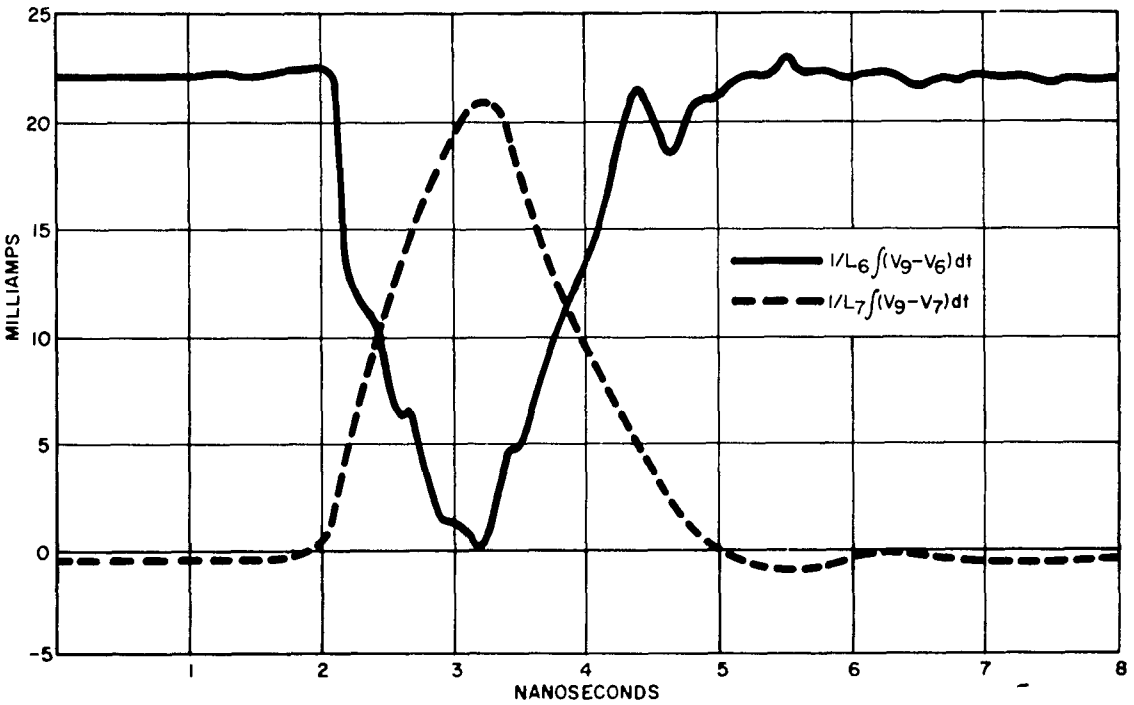


Figure 2-66. Test Circuit Current Waveforms

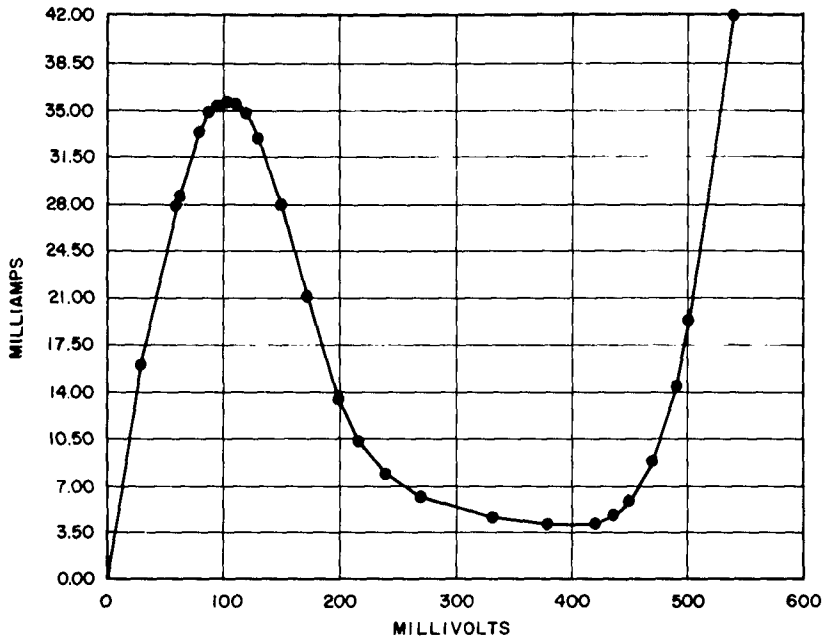


Figure 2-67. Characteristic of 35-ma Tunnel Diode

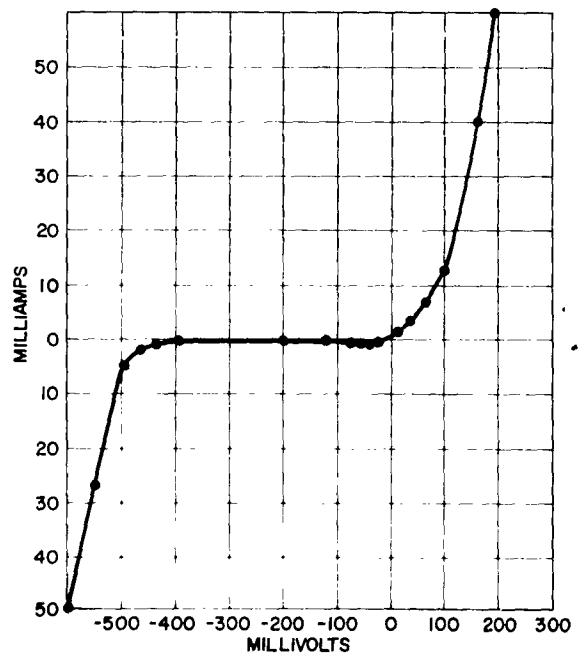


Figure 2-68. Characteristic of 35-ma Clamp Tunnel Rectifier

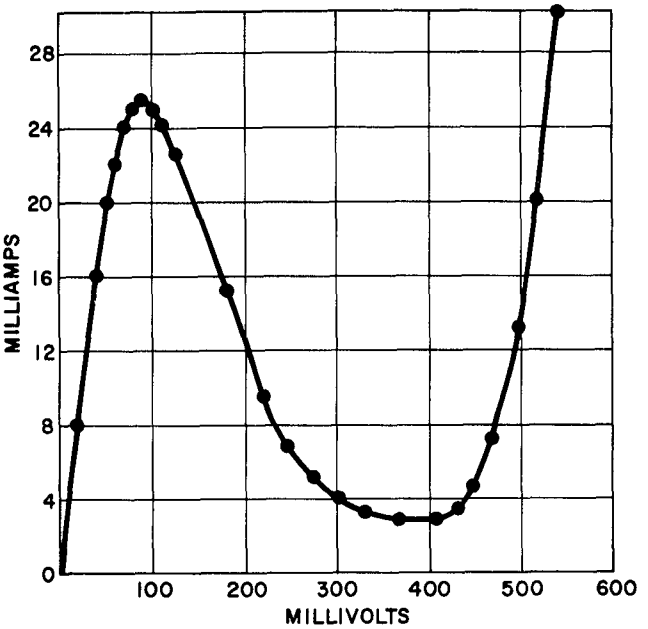


Figure 2-69. Characteristic of 25-ma Tunnel Diode

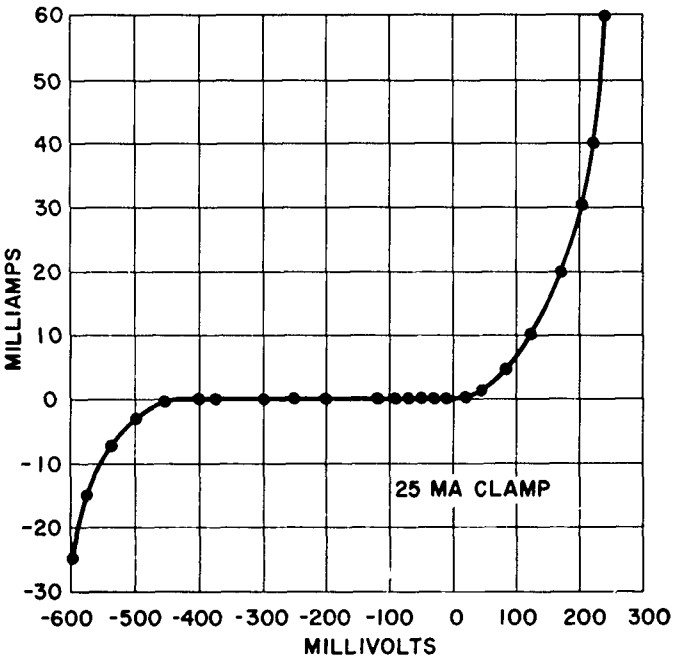


Figure 2-70. Characteristic of 25-ma Clamp Tunnel Rectifier

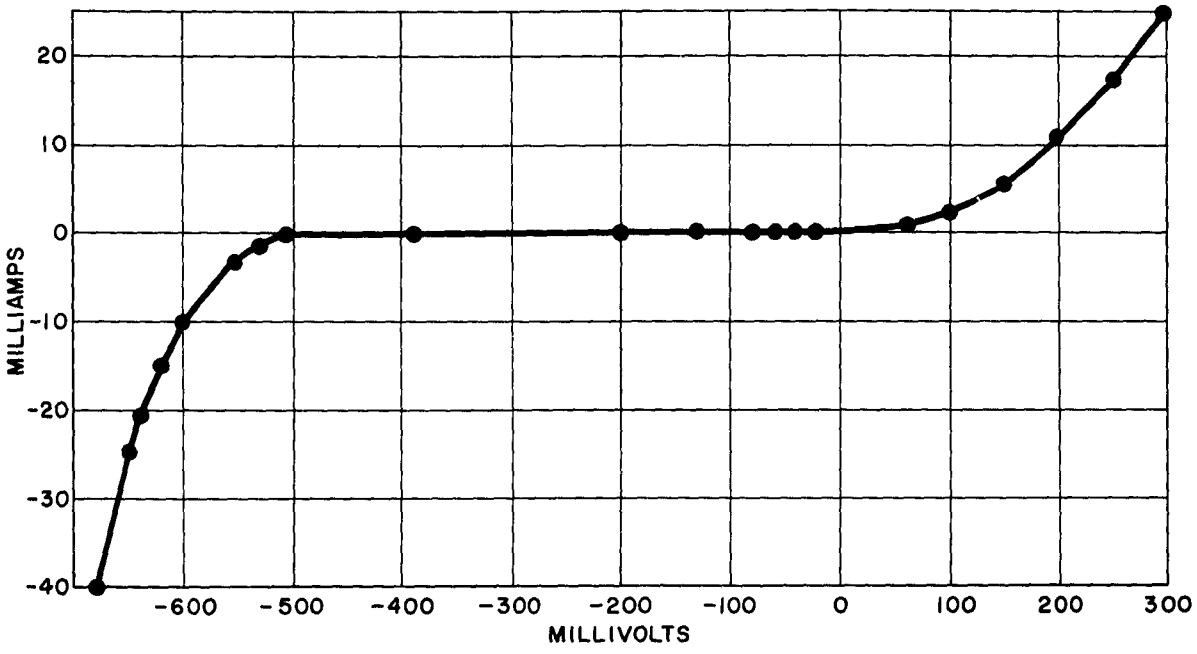


Figure 2-71. Characteristic of 25-ma Coupling Tunnel Rectifier

G. LOGIC INTERCONNECTIONS

Because transmission lines are used in logical interconnectors, some restrictions are placed on the line lengths allowed between circuits. For lines carrying pulses, a maximum length of six inches has been specified for the sybsystem circuits. This limitation is required so that the reflected signal from the loading circuit occurs before recovery of the circuit. If longer lines are required for pulse signals, additional circuits will have to be added along the line. In the case of lines carrying level signals, the line length is dependent upon the maximum rate at which the AND gate at the end of the line is to be activated by its pulse input. The time delay between pulses must be greater than twice the line delay between the bistable circuit and the AND gate. The line places no restriction on the repetition rate of the bistable circuit. The restriction on level carrying lines appears compatible with logic usage since long distance transfers are usually performed at a low repetition rate.

H. GENERAL PROGRAM FOR THE ANALYSIS OF TUNNEL DIODE CIRCUITS

A Fortran program has been written, and is currently being checked, for the simulation of a wide variety of circuits containing tunnel diodes or other non-linear elements. The simulation is performed by the solution of the simultaneous differential equations of the circuit at small time intervals using the Runge-Kutta technique. (Refer to Appendix I.)

The general circuit configuration consists of a rectangular array of nodes and branches as shown in Figure 2-72. Each branch represents a model of a tunnel diode or tunnel rectifier with its non-linear junction characteristic, junction capacitance, series inductance and series resistance. The various elements may be removed so that any branch may contain a resistor, an inductor, a capacitor, or any combination thereof. Furthermore, any branch may be open or shorted. Each node may have a current source, a resistor to ground, or both. The current source can represent a bias or a driving signal having an arbitrary waveform. If the actual circuit uses voltage sources rather than current sources, a simple Thevenin-to-Norton transformation is required.

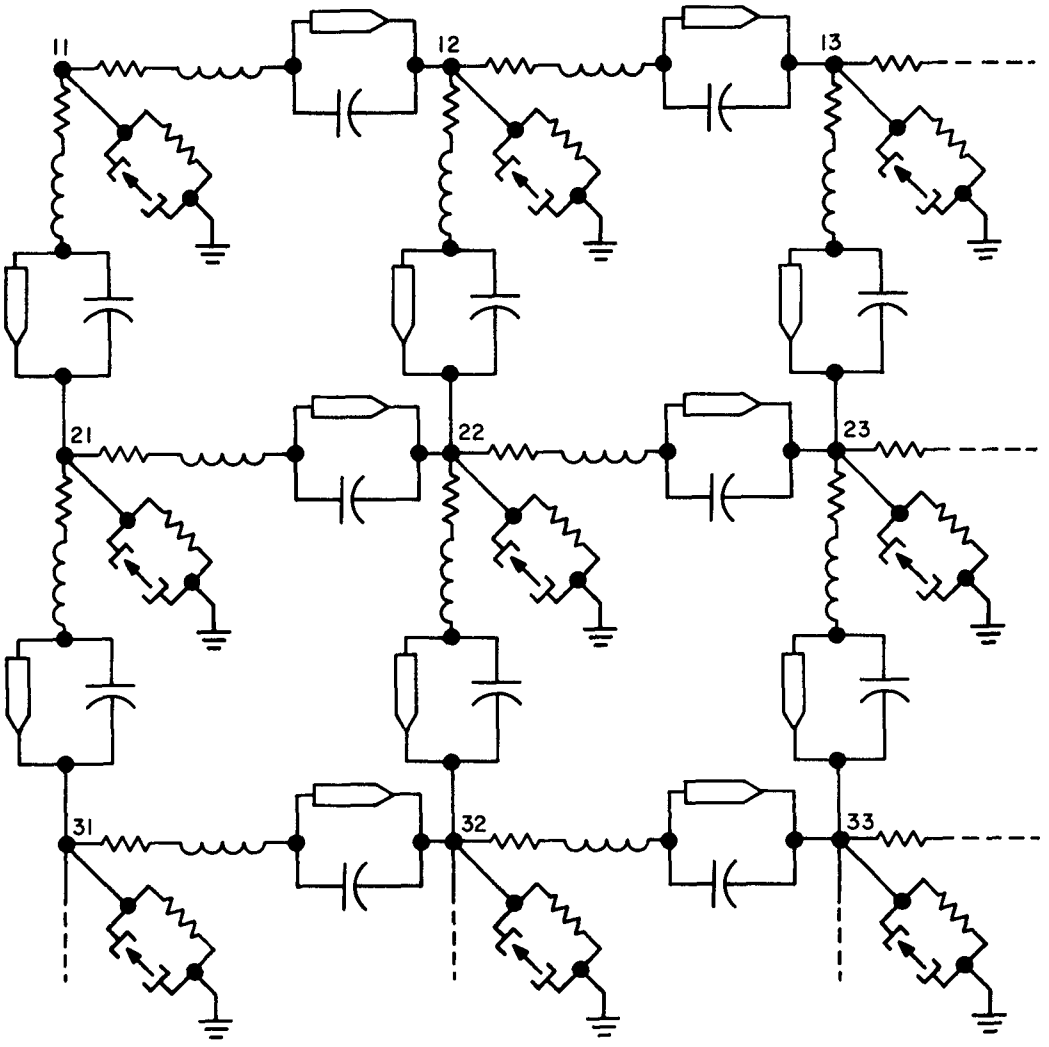


Figure 2-72. General Map for the Solution of Tunnel Diode Circuits

In order to simulate any particular circuit, that circuit must be mapped onto the general rectangular array. The resulting circuit configuration is then defined by specifying the overall size of the rectangular array used, and by describing each branch and node within this array. Each branch is described by giving its type, resistance, inductance, capacitance, diode characteristic, initial junction voltage, and initial branch current. Each node is described by its type, current source, and resistance. The diode characteristics and current sources are described by tables of current vs. voltage and current vs. time, respectively. Other information required consists of the number of rows and columns in the array, the time interval of integration, the total simulation time, and the time interval at which results are to be printed.

The printed results will consist of all node voltages, junction voltages and branch currents at each interval of time. It is also planned to plot certain selected voltages and currents as a function of time.

Chapter 3. FABRICATION

SUMMARY

Refinement of techniques for evaluating tunneling devices was made. The internal inductance of 37 tunnel diodes was measured. Capacity in the 1 picofarad range of several tunnel rectifiers was measured.

Greatly improved speed and accuracy of parameter measurements for miniature coaxial cable was obtained.

A study of the properties of miniature film rod resistors was begun.

An experimental and theoretical study of crosstalk between miniature coaxial cable was begun.

A mathematical study of reflected waveforms on ideal cables was continued.

A component trimming program has been initiated in an attempt to improve the preciseness of some components, and to compensate for the tolerances of other components in order to increase the safety margin and/or the gain of logic system circuits.

Suitable resistors and methods of trimming have been found. Single-stage tunnel-diode circuits have been successfully trimmed and operated at previously chosen power supply voltage levels.

Chapter 3. FABRICATION

I. PERSONNEL

The following personnel contributed to this phase of the project during the eleventh quarter:

I. Abeyta
F. E. Brooks
D. R. Crosby
M. E. Ecker
R. J. Fradette
A. M. M. Hoque
S. T. Jolly
H. R. Kaupp
W. J. Lipinski
E. Luedicke
H. Reinig
D. P. Schnorr

II. DISCUSSION

A. TUNNEL DIODE INDUCTANCE MEASUREMENTS

A test set-up to measure the inductance of a tunnel diode was devised and implemented in the laboratory. This set up is shown in Figure 3-1. All connecting cables have a characteristic impedance of 50 ohms except for the 4-ohm line in the d-c branch of the circuit. This low-impedance line is used to filter out high-frequency disturbances which might leak down from the r-f portion of the circuit. The variable delay line is adjusted to present an open circuit to radio-frequency current. The d-c blocking capacitor prevents direct current from flowing in the r-f signal generator.

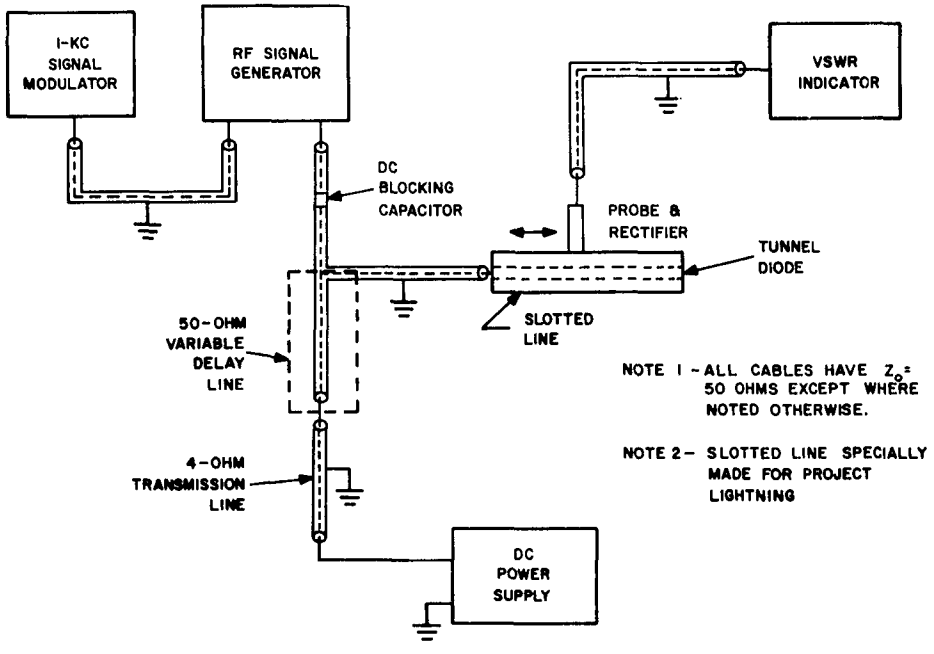


Figure 3-1. Test Set Up for Measuring Tunnel Diode Inductance

The VSWR indicator is tuned to 1 kc to pick up the modulating signal generated by the square wave generator. The d-c power supply is used to bias the tunnel diode in its valley region where the junction capacity of the tunnel diode is known and where the dynamic conductance of the tunnel diode is zero.

Tunnel diode inductance tests were made at frequencies of 2 and 4.2 kmc. Some of the tunnel diodes were tested under valley bias conditions and others were tested with zero d-c bias. Results of this test, the tunnel diodes tested, and certain test conditions are shown in Table 3-1. Various types of tunnel diode packages were tested including the beam and miniature types. Tunnel diodes of 5-, 25- and 50-ma peak currents were tested. Tunnel diode capacitances ranged from 2 to 30 picofarads.

Some of the tunnel diodes were tested twice to indicate the degree of repeatability that could be expected. These values of inductance labelled L_1 and L_2 are for the first and second test, respectively. Repeatability was usually within 20%. The values of inductance measured varied from 0.28 nanohenry to 0.71 nanohenry. However, most of the values fall between 0.4 and 0.5 nanohenry. A total of 37 tunnel diodes were tested. The inductance was determined with the knowledge of the VSWR of a tunnel diode, the shift away from a short-circuit reference null, and a Smith chart. A typical tunnel diode VSWR was about 32 db.

Figure 3-2 shows the equivalent circuit of a tunnel diode. The input impedance of the device is:

$$Z = r + \frac{g}{g^2 + \omega^2 C^2} + j\left[\omega L - \frac{\omega C}{g^2 + \omega^2 C^2}\right] \qquad (1)$$

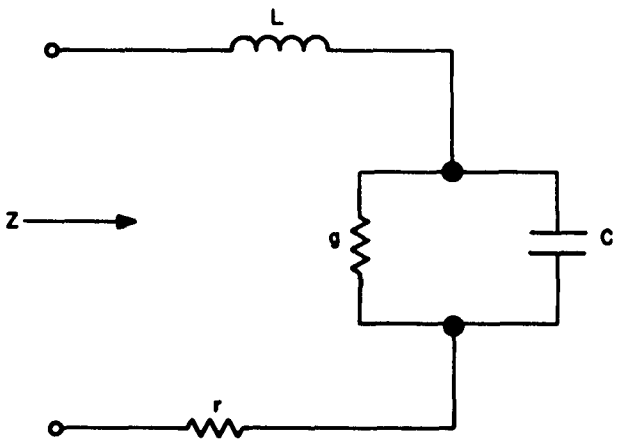


Figure 3-2. Equivalent Circuit of a Tunnel Diode

TABLE 3-1
DATA OF SLOTTED-LINE TESTS

TD No.	I_p (ma.)	C (pf)	D-C Bias	Impedance (ohms)	f (kmc)	L_1 (nh)	L_2 (nh)
7	49.2	17	0	3+j11	4.2	0.42	
130	49.6	19	0	3.2+j15	4.2	0.57	
39	48.8	16	0	2.1+j10.24	4.2	0.39	
30	50.2	16	0	2.35+j11.5	4.2	0.44	
H_1	3.1	2	0	18+j8	4.2	0.30	
14	50	9	0	2+j7.4	2	0.59	
15	50	11	0	2.15+j8.9	2	0.71	
1	5	17.5	0	3.5+j3.5	2	0.28	
2	5	16	0	3+j6	2	0.48	
3	5	24	0	2.5+j5	2	0.40	
4	5	15	0	5+j5.5	2	0.44	
6	4.5	9.5	0	6.25+j6.6	2	0.52	
159	48.2	26	0	1.5+j6.5	2	0.52	
20	53.7	21	0	2.1+j7.5	2	0.60	
4	42	9	VB	1.5+j5	2	0.40	
12	47	30	VB	1.4+j4.55	2	0.36	
13	49	21	VB	1+j5.34	2	0.43	
25	50	18	VB	1+j4.72	2	0.38	
29	50	20	VB	.85+j6.78	2	0.54	
198	51	15	VB	1.5+j6.15	2	0.49	0.4
175	51	15	VB	1.1+j5.49	2	0.44	0.36
159	51	15	VB	1.15+j6.1	2	0.49	0.50
137	51.5	14	VB	1.5+j7.11	2	0.57	
110	51	15	VB	1.3+j5.75	2	0.46	0.43
100	50.5	15	VB	1.15+j5.9	2	0.47	
97	51	15	VB	.65+j4.73	2	0.38	
95	51	15	VB	1.05+j5.56	2	0.44	0.35
82	51	16	VB	1+j5.03	2	0.40	
70	51.5	13	VB	1.1+j6.16	2	0.48	
62	51.5	14	VB	1.04+j5.53	2	0.44	
42	51	13	VB	1.4+j5.26	2	0.42	0.52
36	51	15	VB	1.45+j4.77	2	0.38	
33	51.5	14.5	VB	1.2+j5.49	2	0.44	0.46
75	49.5	13	VB	1.45+j5.96	2	0.47	0.42
16	26	6	VB	2.35+j3.74	2	0.30	
8	26	6	VB	2.3+j4.05	2	0.32	
14	25	6	VB	1.25+j4.6	2	0.37	

With valley bias, g becomes zero and (1) becomes:

$$Z = r + j\left[\omega L - \frac{1}{\omega C}\right] = r + j\,X \qquad (2)$$

The value of X is obtained from a Smith chart. Since the diode capacity is known accurately in the valley, $\frac{1}{\omega C}$ can be computed and added to X to find ωL. With ωL known, the inductance, L, of the tunnel diode can be computed. For the dynamic conductance in the valley to remain essentially zero, a small r-f signal must be used to drive the tunnel diode, For the tests, 5 mv peak-to-peak was used. With this signal level, the VSWR indicator must be operated in its most sensitive range where the background noise level makes the null and peak of the standing wave difficult to locate.

Another area of difficulty was the lack of stability and repeatability in the connections of the tunnel diode to the slotted line.

B. TUNNEL DIODE PEAK AND VALLEY CURRENT MEASUREMENT

A test jig was designed, constructed and tested in the laboratory for measurement of these parameters. The schematic diagram of this jig is shown in Figure 3-3.

In this test jig, the 0.6-ohm resistor in series with the tunnel diode samples the current that flows through the tunnel diode under test, as the voltage developed across this resistor is proportional to the diode current. The peak current and valley current of the tunnel diode is reached when the voltage across the sampling resistor is a maximum or minimum, respectively. It is desirable to be able to sweep some amount of

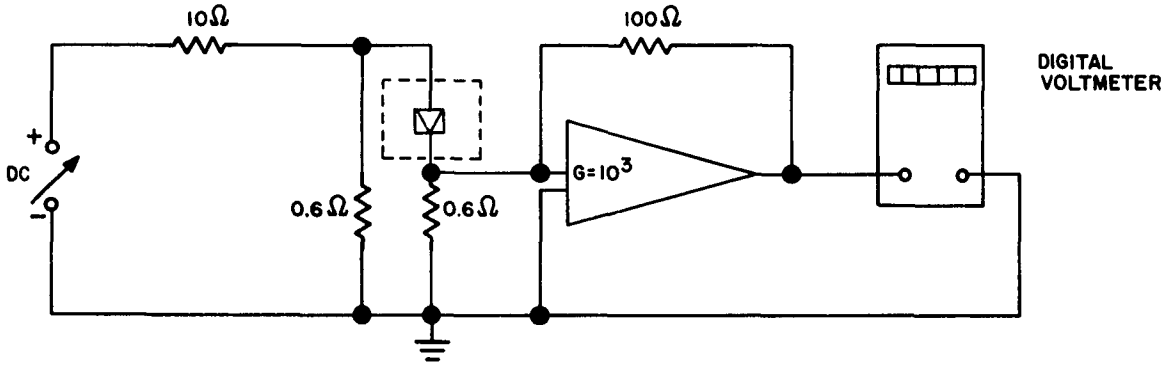


Figure 3-3. Schematic Diagram of Test Jig for Measuring Peak and Valley Currents

voltage across the knee and valley of the tunnel diode V-I curve, to enable pinpointing the peak and valley exactly. Since excursion across the peak and valley means entry into the negative-resistance region of the V-I curve, attention must be paid to the stability of the tunnel diode circuit. To prevent switching from the low to the high state, the equivalent series resistance, R_S, that the tunnel diode sees must be less than the smallest negative resistance, R_n.

$$R_S < R_n \tag{3}$$

To prevent oscillations the L_S/R_S time constant must be less than the R_nC time constant of the tunnel diode, where L_S is the total series inductance and C is the capacitance of the tunnel diode junction.

$$\frac{L_s}{R_s} < R_nC \tag{4}$$

For the test jig under discussion, the value of R_S is about 1 ohm. The 0.6-ohm resistors are placed close to the body of the tunnel diode to obtain a low inductance path around the tunnel diode. The inductance of this circuit is difficult to determine; it is estimated at 1.5 nanohenries, including the inductance of the tunnel diode.

Equation (4) can be manipulated to obtain $\frac{L_S}{R_nC} < R_S$. Combining this with (3) yields:

$$\frac{L_S}{R_nC} < R_S < R_n \tag{5}$$

Relation (5) becomes:

$$\frac{L_s}{R_n C} < R_n \tag{6}$$

And relation (6) now becomes:

$$R_n > \sqrt{\frac{L_s}{C}} \tag{7}$$

Using the value of L_S mentioned above and assuming a capacitance of 15 pf, it is determined that if $R_n > .10$ ohm the circuit will be stable. Reference to a typical V-I curve for a tunnel diode shows a point in the negative-resistance region close to the peak corresponding to 10 ohms resistance. Beyond this point the circuit will oscillate. In the laboratory, several specimens were tested and reasonable results were obtained as shown in Table 3-2. Using a power supply with fine control of the output voltage enabled reaching a point just slightly beyond the peak of the tunnel diode before oscillatory effects were noticed. The valley was easier to monitor because the V-I curve in this region is flatter than at the peak.

TABLE 3-2
PEAK CURRENT TEST RESULTS

TD No.	RATED		TESTED
	Ip (ma)	C (pf)	Ip (ma)
14	50.0	9	49.2
137	51.5	14	50.1
159	48.2	26	46.9
6	4.5	9.5	4.1
20	53.7	21	52.7

A d-c amplifier was used to boost the small voltage produced across the sampling resistor to enable the electronic digital voltmeter to operate near its mid-range where the instrument is more accurate. This amplifier has an open-loop gain of about 10^3 and is a high input impedance instrument with a range of 0.1 mv to 1000 mv. The accuracy of the resultant current values depends mainly upon the preciseness of the electronic voltmeter which is better than 0.1%.

The 0.6-ohm resistors used were deposited carbon on a ceramic substrate in the form of a rod. The 10-ohm resistor was used to isolate the power supply from the test circuit.

C. TUNNEL RECTIFIER CAPACITY MEASUREMENTS

The laboratory set up used to measure tunnel rectifier junction capacity is essentially the same as that used for tunnel diodes; however, greater absolute accuracy is required to measure the small capacities associated with the tunnel rectifier. The capacity measuring set up is shown in Figure 3-4.

The old jig used to measure tunnel diode capacity is shown in Figure 3-5 (left side). To take a measurement using this jig, the bridge is first balanced with the diode removed from the jig or holder. Then the diode is inserted and the bridge is rebalanced. However, on initially balancing the bridge some of the capacity that should be associated with the tunnel diode is balanced out. This fact is best illustrated by imagining an attempt to measure a capacitor which has the same dimensions as its holder.

The second jig, shown in Figure 3-5 (right side), not only minimizes this effect but also simulates an actual circuit wafer. This jig yields a capacity value of 0.1 picofarad higher than the old jig -- a significant difference since some tunnel rectifiers have capacity values of less than 1.0 picofarad.

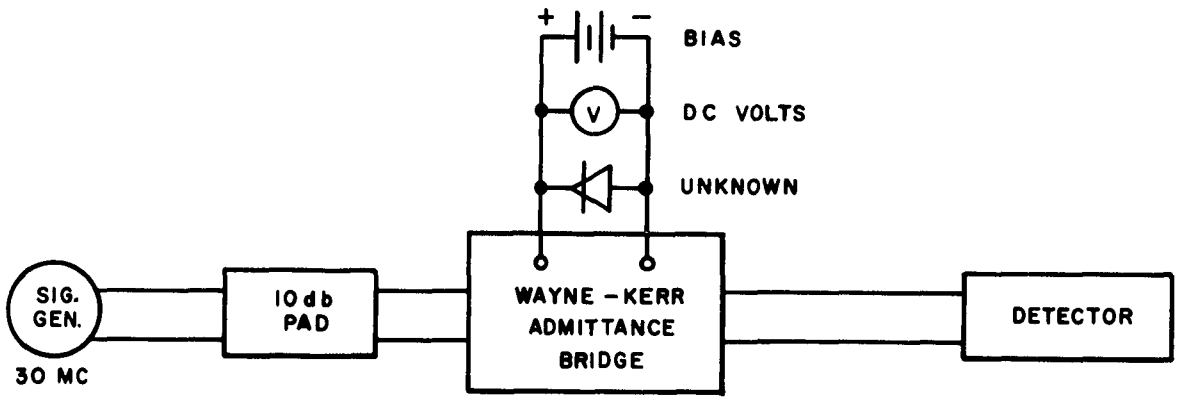


Figure 3-4. Tunnel Diode Capacity Measurement Set Up

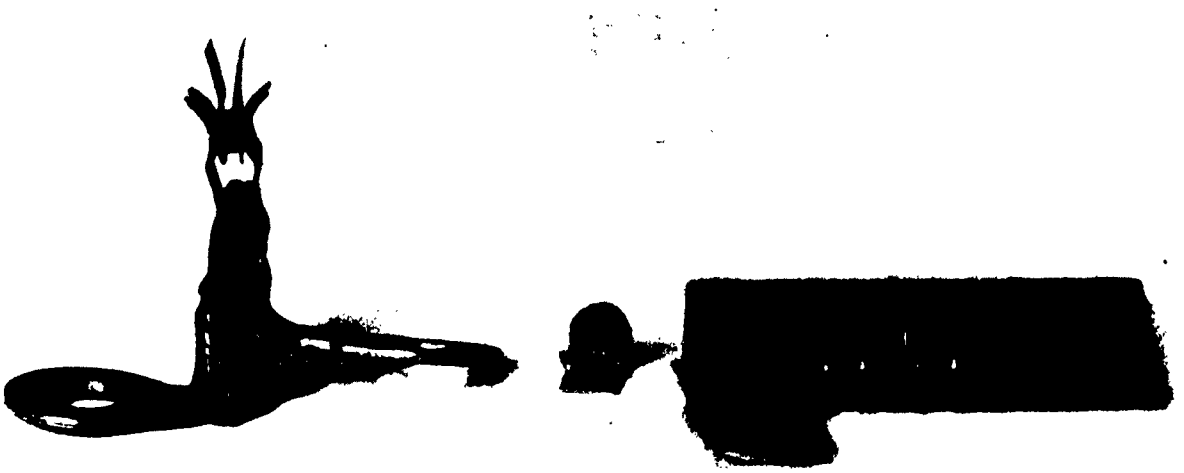


Figure 3-5. Jigs for Tunnel Rectifier Capacity Measurement

Measurements were made using an a-c voltage swing of approximately 6 millivolts across the rectifier. The equivalent circuit of the rectifier is represented in Figure 3-6. Both the conductance, g, and the capacity, C, are functions of d-c bias voltage.

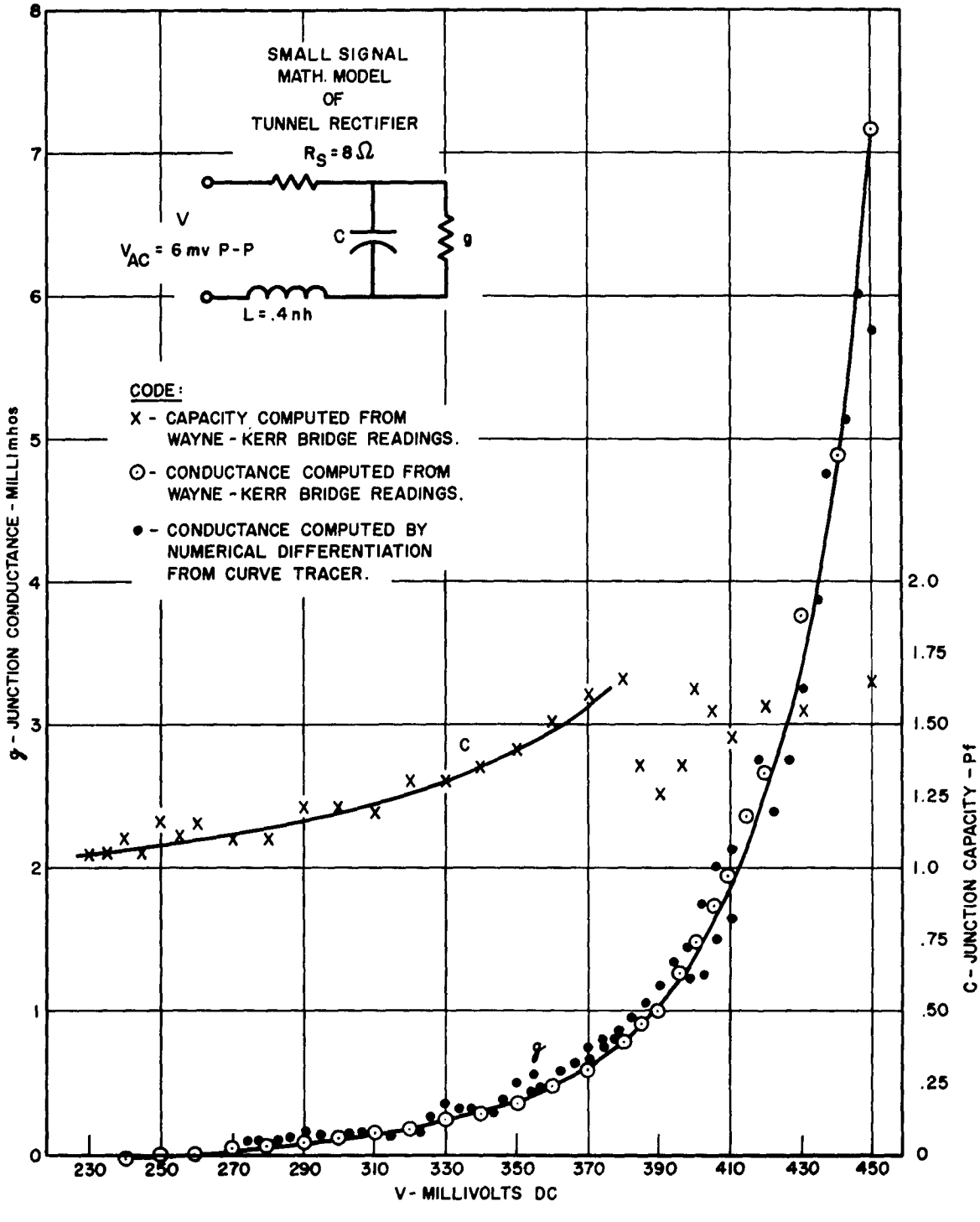


Figure 3-6. Measured Tunnel Rectifier Parameters

The small signal admittance of the rectifier is,

$$Y_d = \frac{1}{R_s + i\,\omega\,L + \frac{1}{g + L\,\omega\,C}}$$

separating Y_d into its real and imaginary components

$$Y_d = \frac{[g + R_s\,(g^2 + \omega^2\,C^2)] + i\,[\omega C - \omega L\,(g^2 + \omega^2\,C^2)]}{(1 + R_s g - \omega^2 CL)^2 + \omega^2\,(R_s\,C + gL)^2}$$

For the rectifier admittance to equal the indicated bridge admittance, R_s and L must include any resistance and inductance associated with the jig.

Parameter values for RCA tunnel rectifiers are in the following ranges;

$$-1 < g < 1 \quad \text{mhos}$$

$$10^{-10} < L < 10^{-7} \text{ henries}$$

$$10^{-13} < C < 10^{-11} \text{ farads}$$

$$1 < R_s < 10^2 \quad \text{ohms}$$

The frequency at which the measurements are made is 30 mc.

Using the ranges of parameter values cited above, conservative approximations for the tunnel rectifier junction capacity and conductance are:

$$g = \frac{G}{1 + R_s G}$$

$$C = B + 2R_s gB + g^2\,(R_s\,B + L)$$

where G and B are the conductance and capacity values as read on the admittance bridge.

It can be seen from the above equations that when the tunnel rectifier is biased in the valley of its characteristic ($g = 0$), the bridge indicates the junction capacity directly.

Table 3-3 compares this value of capacity with that specified by the RCA Semiconductor and Materials Division, who supplied the rectifiers tested.

Data on tunnel rectifier unit #121 was taken with a bias range of 240-450 millivolts. The series resistance, R_s, was calculated from the slope of the non-linear characteristic at -20 ma as 8 ohms. Tunnel rectifier inductance was assumed to be 0.4 nanohenry, while the inductance of the jig and internal bridge leads were found to be approximately 43 nanohenries. Junction capacity and conductance as computed from the bridge readings are plotted in Figure 3-6.

TABLE 3-3
COMPARISON OF CAPACITY MEASUREMENTS

Unit No.	134	130	141	121	32
Valley Voltage (mv)	255	280	220	250	280
Measured Capacity (pf)	1.5	1.3	1.3	1.1	3.2
Rated Capacity (pf)	1.3	1.3	1.2	1.0	3.2

The conductance was also computed using a picture taken from the curve tracer. The plot of this measured conductance is shown in Figure 3-6. Many points were computed to compensate for the inherent inaccuracy in reading data from the curve tracer picture.

The capacity curve in Figure 3-6 is not as anticipated for bias voltages above 380 millivolts. The capacity should continue to increase asymptotically approaching infinity at some finite bias voltage of less than one volt. The bridge readings in the questionable region were rechecked and found to be substantially correct. At present, there is no explanation for this phenomenon.

The smallest division of the admittance bridge capacity dial is 1.0 picofarad; however, the dial resetability is better than 1.0 picofarad. In the near future, a variable calibrated capacitor will be utilized in the set up to eliminate the human error in reading capacity values to 0.1 picofarad.

D. COAXIAL TRANSMISSION LINE

Two types of miniature coaxial transmission line were tested. Both types had a core of teflon insulated copper wire. The preferred type uses drawn tubing as its outer conductor while the other has a deposited metallic conductor. The drawn line is preferred due to its lower losses, smooth surface, lack of cracks and checks, and general ruggedness.

1. Losses

Loss measurements have been made on various impedances, diameters, and materials of both line types. Figure 3-7 shows losses in db per foot for different classes of drawn line, while Figure 3-8 shows losses for a deposited line. It should be noted that theoretically, losses vary inversely with diameter and characteristic impedance. Comparison of deposited and drawn lines of similar impedances and diameters shows the basic difference in losses between these types.

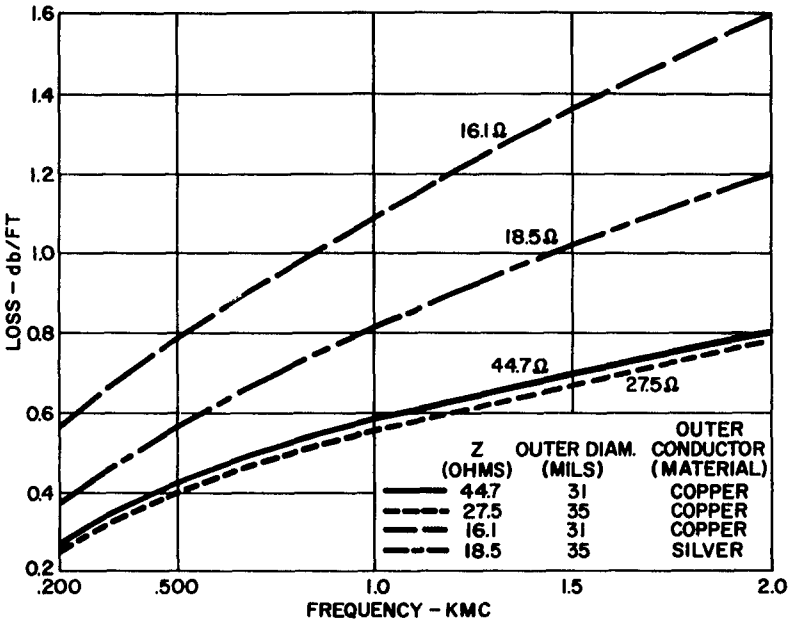


Figure 3-7. Attenuation of Cable with Drawn-Metal Outer Conductor

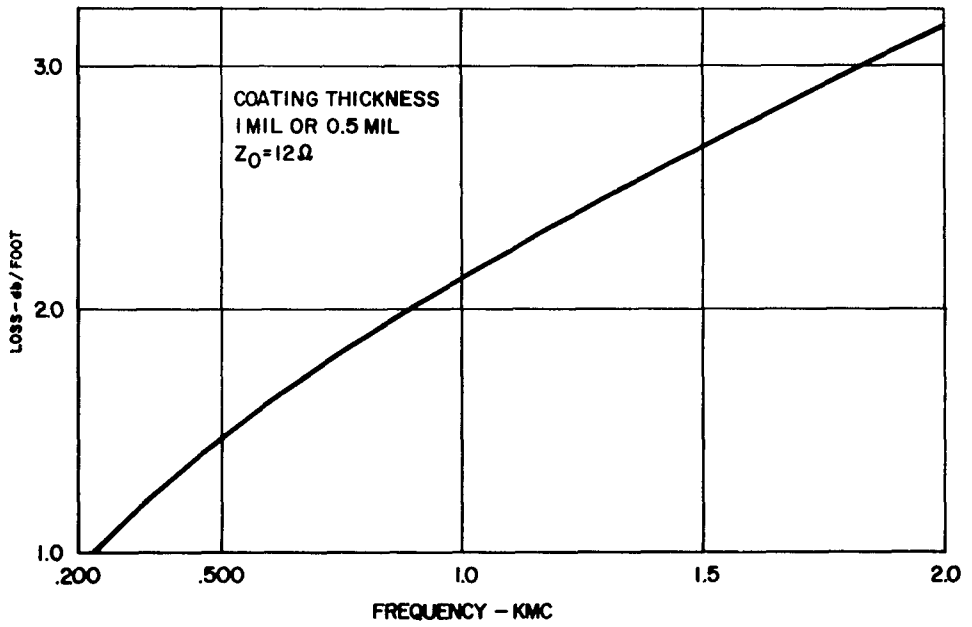


Figure 3-8. Attenuation of Cable with Deposited-Metal Outer Conductor

The losses in these transmission lines vary as the square root of frequency and agree fairly well with calculated conductor losses. This indicates that virtually the losses are all due to conductor resistance with no dielectric losses in the teflon insulation.

2. Characteristic Impedance

Characteristic impedance is the other important parameter of transmission lines. Characteristic impedance value must be held to 5% or better, making the mechanical dimensions of the line quite critical. Z_o is given by the following formula:

$$Z_o = \frac{138}{\sqrt{\epsilon}} \log \frac{D}{d}$$

where

ϵ = dielectric constant

d = diameter of inner conductor

D = outer diameter of insulation

Tentatively, d can be held to ±0.1 mil and "D" to ±0.5 mil. Figure 3-9 is a plot of tolerance vs. Z_o for these mechanical variations.

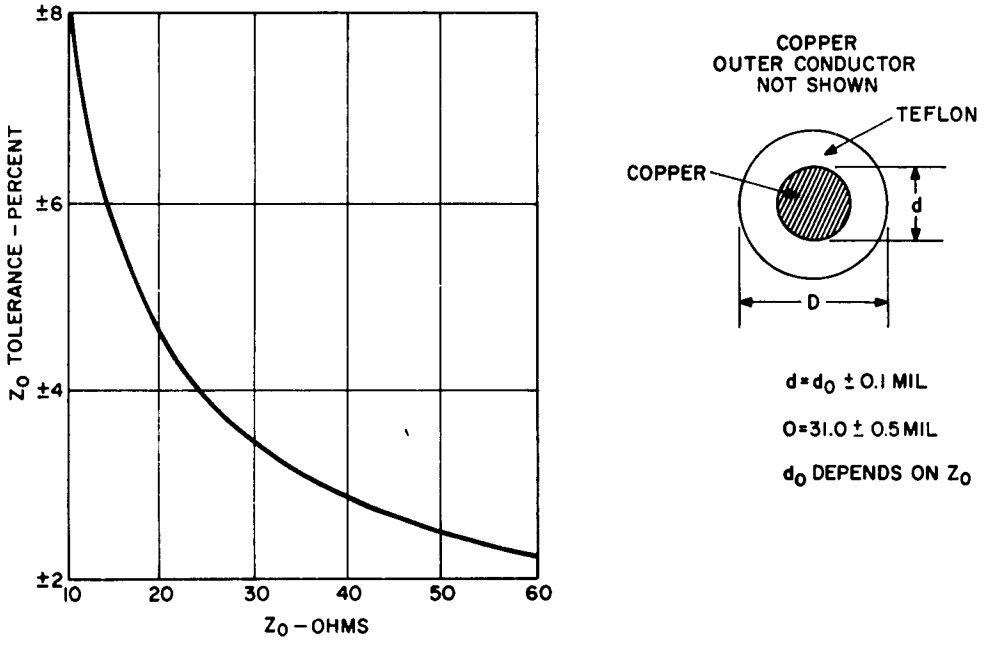


Figure 3-9. Tolerance on Z_o for Fixed Mechanical Variations

The Z_o is also affected by decentering of the center conductor. An increase in tolerance of ±0.5% may be necessary to allow for this variation.

3. Characteristic Impedance Measurements

Z_o for a piece of transmission line is determined by two characteristics.

(a) Capacitance

(b) Velocity of Propogation or Resonant Frequency

Accurate capacitance measurements are possible due to the nature of the teflon dielectric. Since losses in teflon are very low and its frequency stability is practically ideal, measurements are not influenced by frequency of the measuring equipment or losses in the transmission line.

Measurements of capacity are made using a Q-meter in conjunction with a precision variable capacitor. Capacity substitution is employed to eliminate lead and fixture capacitance. Use of a relatively low frequency (500 kc) eliminates transmission-line and lead-inductance effects.

The accuracy of these capacity measurements is better than 0.75%.

4. Resonant Frequency Test

The object of the resonant frequency test is to find the half wavelength frequency of a piece of coaxial line and thus the velocity of propogation. At resonance, the apparent impedance looking into an open section of line is a pure resistance; and in the vicinity of this frequency, the impedance performs like a parallel resonant circuit. Using these facts, apparent impedance is measured and the frequency is changed until the impedance looks purely resistive. The frequency thus obtained can be checked by use of a crystal calibrator or counter. Accuracy of this measurement is better than 0.75%.

The Z_o of a piece of transmission line can be calculated from these two parameters by the following formula.

$$Z_o = \frac{1}{2fC}$$

where:

C = capacity of line

f = 1/2 wavelength frequency of line

It should be noted that line length does not enter into the above calculation. Consequently, the length of line is not a source for error in these measurements.

Sources for error in these capacity measurements are mainly from the standard capacitor and the ability to repeat Q-meter peaking. The errors in the resonant frequency measurement come from fringe fields around the line, possible oscillator frequency shift after calibration errors in reactance readings, and discontinuities at the connection between the impedance meter and the transmission line.

Data is being taken on large numbers of line pieces to determine production type variations. Although absolute accuracy is about ±1.5%, relative comparisons should be accurate to about ±0.5%.

5. Line Chopping Test

The second method for measuring line velocity is a destructive test for which the lab set up is shown in Figure 3-10. Small segments of line are removed and the probe voltage read at each removal. The standing wave pattern can then be plotted considering the voltages and the line lengths removed. The effective dielectric constant can be computed from the wavelengths:

$$\sqrt{\epsilon} = \frac{\lambda_a}{\lambda_\ell}$$

where:

ϵ = dielectric constant

λ_a = wavelength of test frequency in air

λ_ℓ = wavelength of test frequency in line.

and

$$Z = \frac{833\sqrt{\epsilon}}{C_i}$$

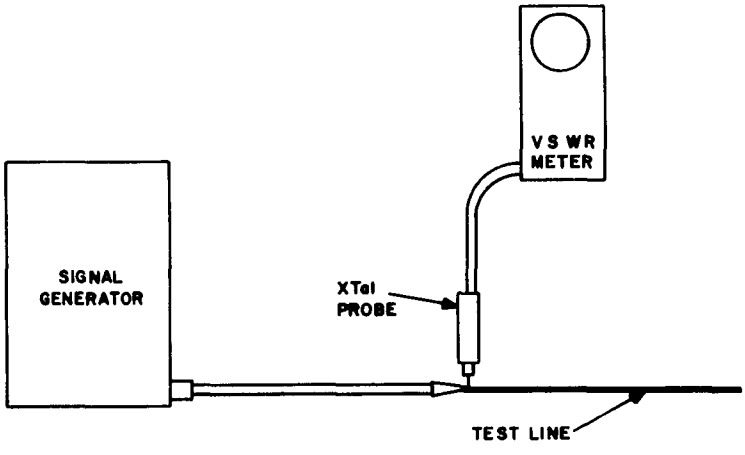


Figure 3-10. Set Up for Line Chopping Tests

where:

C_i = capacity in pf/inch

The accuracy of this method is dependent upon the measurement of line length removed and the frequency measurement. Errors due to fringing and reactances in connections are eliminated.

6. Computer Program

To verify the line chopping method, a computer program was run using the equivalent circuit shown in Figure 3-11. Points were computed and plots made of probe voltage vs. line length. The plots made were for various values of probe reactance and various characteristic impedances of the test line. The attenuation parameter used was based on experimental loss data, with the phase shift being based on a teflon dielectric of 2.08.

Comparison of experimental points with a selected computed curve is shown in Figure 3-12. Correlation between these two is generally quite good. The computed curve selected had a test line impedance of 46 ohms and an assumed probe reactance of 12 ohms.

The effect of probe reactance changes upon the theoretical waveform and the effect of different test line impedances are shown in Figures 3-13 and 3-14, respectively.

The experimental data (Figure 3-12) agrees quite well with the calculated data, indicating that the line chopping test is reliable. Comparisons between this data and the resonant frequency test, previously described, also show agreement between the two methods. Thus, the accuracy of the resonant frequency test is substantiated.

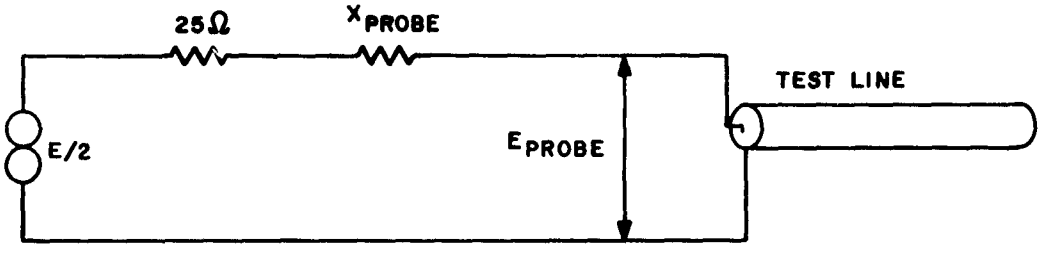


Figure 3-11. Equivalent Circuit of Line Chopping Test

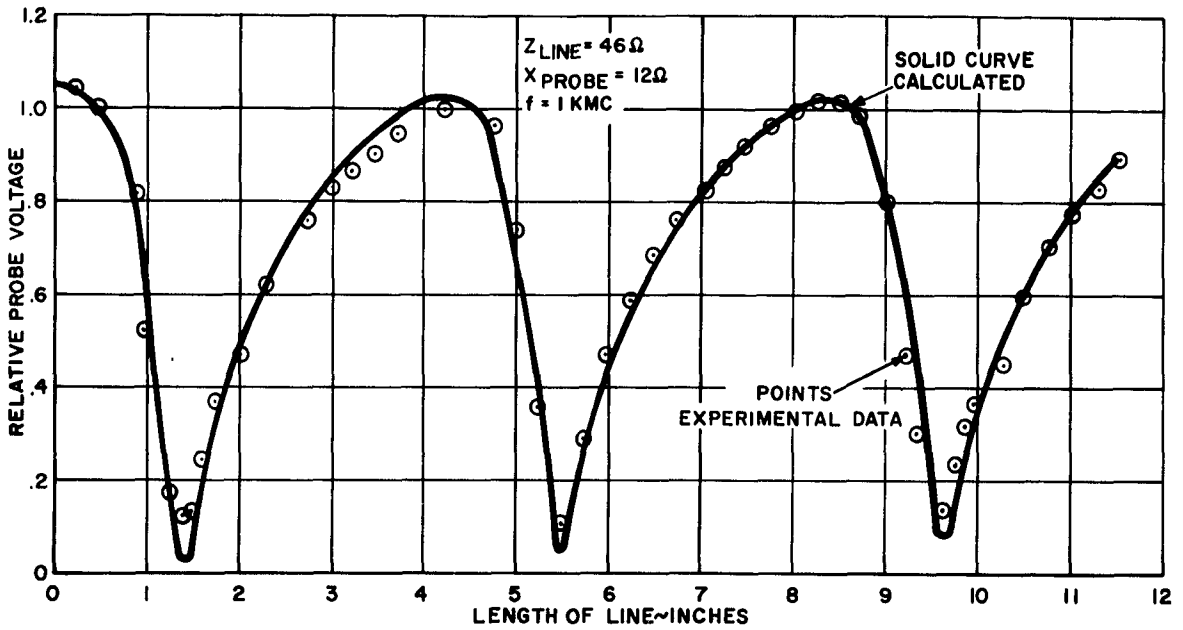


Figure 3-12. Experimental and Calculated Probe Voltage vs. Line Length

7. Line Velocity Test Comparison

In general, the resonant frequency test is preferable to the line chopping test. Relative merits are shown in Table 3-4 below:

TABLE 3-4
LINE VELOCITY TESTS

Feature	Resonant Freq. Test	Line Chop Test
Absolute Error	±0.75%	±0.75%
Destructive	No	Yes
Ease of Testing	Good	Poor
Comparative Error*	±0.25%	±0.75%
*Relative Measurements between different pieces		

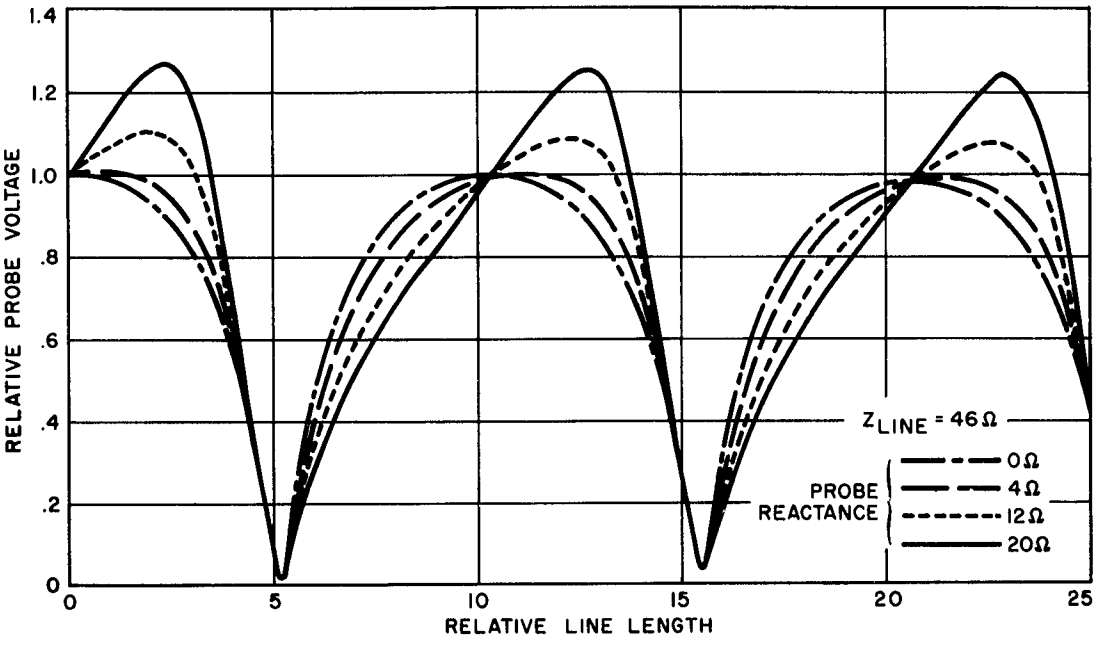


Figure 3-13. Calculated Probe Voltage vs. Line Length with Probe Reactance a Parameter

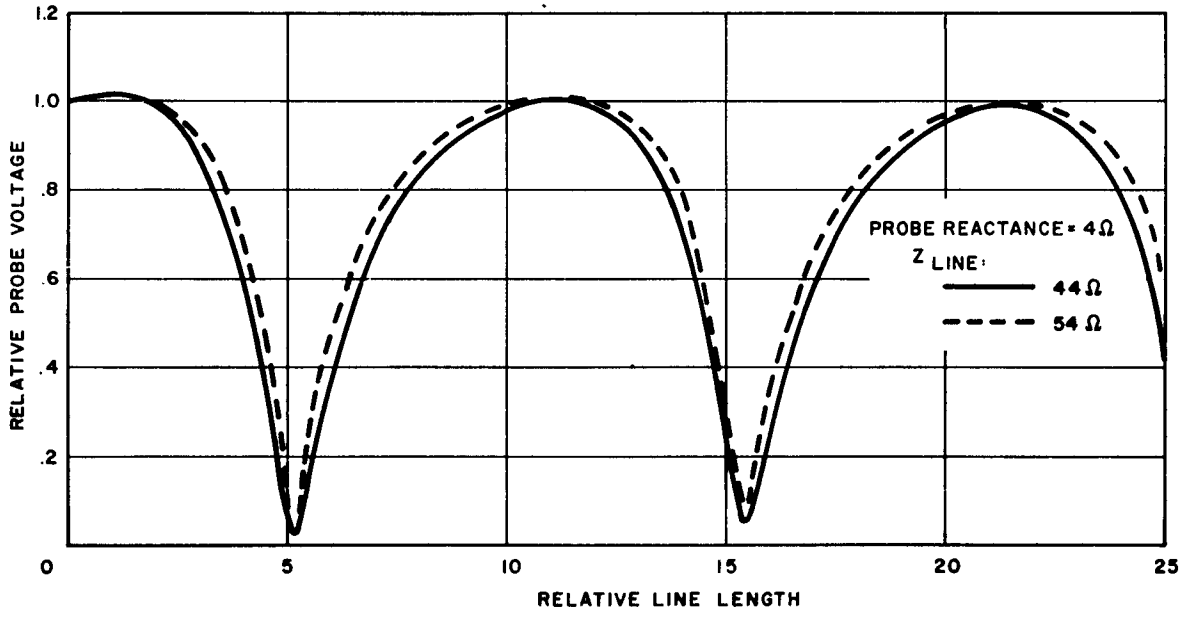


Figure 3-14. Calculated Probe Voltage vs. Line Length with Line Impedance a Parameter

8. Large Scale Measurements

Refinements of the resonant frequency method have been made to expedite large-scale testing. Initial tests on 24 sections of 17-ohm line show a variation of ±1.7%, which is well within the limits shown in Figure 3-7.

E. COAXIAL CONNECTOR

1. Channel Type

Various line-to-line coaxial connectors are being considered. The best type under test so far is a solder type. This connector can be used for several pairs of miniature transmission lines and employs soldered joints for both outer and inner conductors. Due to the small mechanical dimensions and the solid-walled outer connector, the drawn type coax can be readily soldered.

The ground circuit path and the mechanical foundation for the unit are provided by a channel member. The insulation is fastened inside the channel. Individual cables can be installed and removed easily.

The discontinuity caused by the connector is kept to a minimum by proper selection of insulation thickness and strip width to match the coaxial line being used.

2. Transient Connector Test

A test system for transient evaluation of connector discontinuities is shown in Figure 3-15. A relatively wide pulse is formed at the pulse generator (50 ns duration). This can be considered as a step for the time duration involved here. This step is launched down the transmission line. First the incident wave strikes the scope, followed

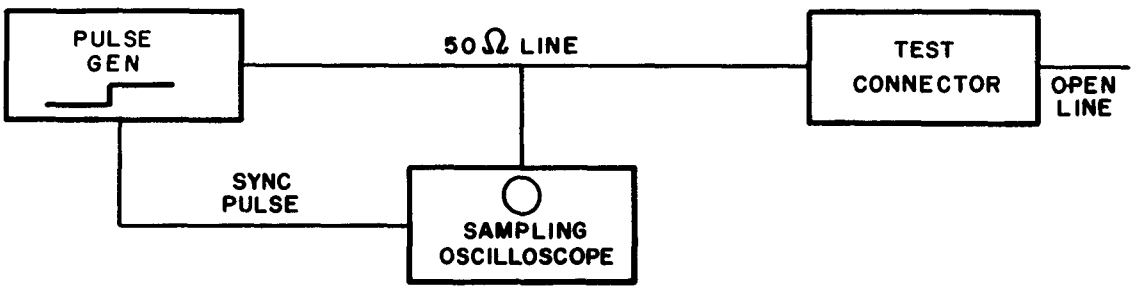


Figure 3-15. Set Up for Transient Connector Test

by a reflection from the connector under test and finally by the reflection from the end of the line. In this manner, the connector reflection is isolated in time from other system discontinuities.

Mathematically, it can be shown that effective reactances in a smooth line will reflect pulses when the incident waveform is a step. An inductive discontinuity reflects a positive pulse and a capacitive discontinuity a negative pulse. The width and amplitude of the reflection can be used as a measure of the connector's transient performance.

In the test system being used, the viewable risetime of the incident step is 0.7 ns. Preliminary results show the connector to have a pulse reflection amplitude of 1% of the incident step.

The accuracy of this method is rather limited. Electrical noise and oscilloscope inaccuracies are limiting factors. However, computer waveforms are transient in nature, and an evaluation of this type is more significantly relative to actual operation than a steady state test.

3. Steady State Test

A possible approach to steady state connector measurement has been indicated by the computer plots of Figure 3-13, which shows the effect of reactance upon a variable-length transmission line. Since reactance has a distinct and predictable effect on the waveform encountered, a converse approach of evaluating the reactance from the waveform appears in order. Preliminary measurements indicate that this approach may be satisfactory.

4. Connector Crosstalk

Values of steady state crosstalk of -50 db between two adjacent connections have been obtained. Connector crosstalk will be evaluated in both steady state and transient conditions; pulse crosstalk will also be evaluated.

F. DELAY LINES

Design of a passive delay line is being undertaken. The requirements are as follows:

(1) Z_o = 25 ohms

(2) Delay = 20 ns

(3) Risetime = 1 ns

In general, the ratio of risetime to delay is the figure of merit of a delay line.

1. Lumped Parameter Type

One approach to a delay line is the use of discreet inductances and capacitances. This approach is being investigated using printed techniques and a low-loss, low-dielectric material, teflon. Calculations show that for the required figure of merit 20 to 100 sections are required.

2. Distributed Type

The distributed delay line uses a high-dielectric material to obtain delay. Tests have been made on a barium-titanate material with a dielectric constant of 1000. The resultant delay time was 19 ns, but an unsatisfactory risetime of 15 ns accompanies this delay. This excessive risetime is due to high-frequency losses in the dielectric. Steps are being taken to obtain better dielectric materials and improved line configurations.

3. Testing Delay Lines

The test set up for delay lines is shown in Figure 3-16. A fast risetime step is fed into the system. Excluding the delay line, the system risetime is 0.7 ns. The step voltage is viewed as it comes through the delay line and the risetime can immediately be measured on the oscilloscope. In addition to this direct transmission, a secondary reflection is obtained from this connection at the generator side of the delay line. This reflection appears on the oscilloscope after the initial step. The delay of this reflection is twice the delay time of the line. Thus, one waveform is used to evaluate both delay time and risetime.

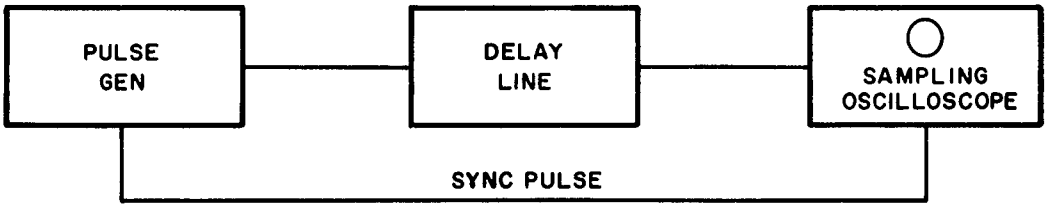


Figure 3-16. Set Up for Delay Line Test

G. RESISTORS

The miniature film rod resistors, 0.120-inch long, used for the developed circuits are relatively new on the market, and as such must be evaluated to determine their capabilities and limitations relative to these circuits.

Tests made for the evaluation of these resistors consisted of (1) physical inspection; (2) resistance measurements on a Wheatstone Bridge, as received from the manufacturer, after soldering to test set up; (3) resistance measurements under various loads by the voltage comparison method using resistors of comparitively larger wattage rating as standards; (4) extended life test at 100% rated load.

A lot of 94 resistors from our principal supplier were evaluated on the basis of the above test. Of the 94, 12 were initially rejected for being out of the ±1% tolerance, 21 rejected for going out of tolerance after soldering and 11 were rejected for going out of tolerance after a 72 hour life test at rated loads.

Some trouble had been experienced in the handling and soldering of the resistors. Subsequential developments of special tweezers with teflon jaws and split soldering iron tips show promise of eliminating the handling and soldering problems. Close cooperation on the part of the manufacturer is encouraging in cutting down the number of initial rejects.

Continued and improved evaluation tests are to be conducted on a sampling of the resistors received from the vendor.

H. COAXIAL CABLE CROSSTALK MEASUREMENTS

Before examining the crosstalk associated with the miniature coaxial cable used in the subsystem, some crosstalk measurements were made on commercial cable.

Two one-meter lengths of RG58 C/U coaxial cable were used in the tests. A schematic of the test set up appears in Figure 3-17. The outer conductors of the cables are connected only at the terminations. The inner conductors are not completely shielded in the last two centimeters at each end of the cable.

Data was recorded for different parallel spacings of the cables; however, the spacing at the terminations was fixed at 2.54 cm. Three cases of spacing were considered.

(1) The cables spaced 2.54 cm apart.
(2) The cables taped together throughout their length, separated only by their outer insulation (spacing 0.12 cm)
(3) The outer conductors of the cables soldered together throughout their length.

The results are indicated by the plots of crosstalk ratio vs. frequency in Figure 3-17. Limitations of the test equipment prevented measuring crosstalk ratios below 85 db. The highest frequency at which measurements were recorded in Figure 3-17 was 20 kc. One wavelength of RG85 cable is 10^4 meters long at 20 kc, thus the test set up may be considered a lumped circuit for the data in the figure.

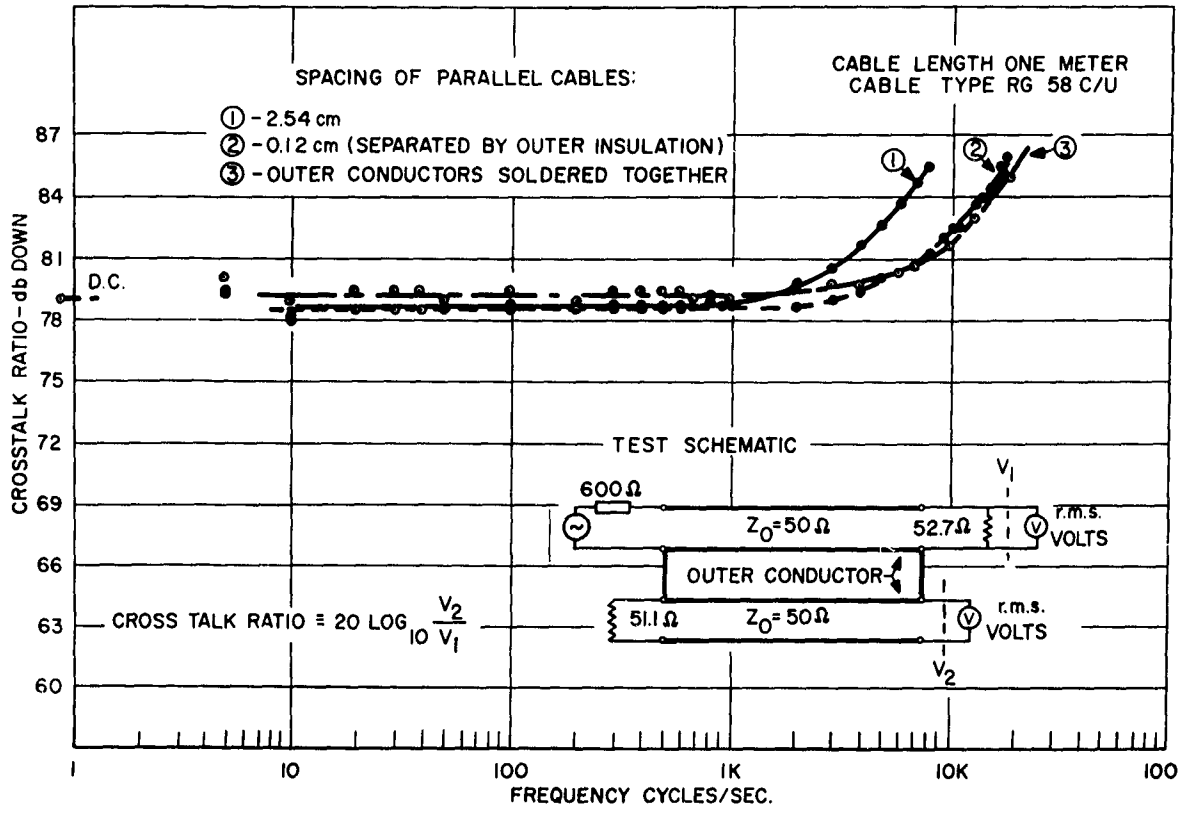


Figure 3-17. Measured Crosstalk Between Cables

The result of extending case (3) above to higher frequencies is shown in Figure 3-18. It is seen that the crosstalk ratio decreases sharply between 0.2 and 10 mc. This phenomena is caused by the relatively poor grounding and lack of shielding at the terminations. Although cases (1) and (2) are not shown at higher frequencies the results are similar to case (3).

The results of improved grounding while shielding the inner conductors are shown in Figure 3-19. The effect is to reduce the crosstalk at frequencies above 3 kc.

Upon terminating the cables in conventional panel-type coax fittings, no crosstalk was evident from 10 kc up to 10 megacycles.

Considering the close proximity and the short lengths of coaxial cables in the proposed subsystem, it seems the most severe crosstalk will appear at the terminations on the wafers.

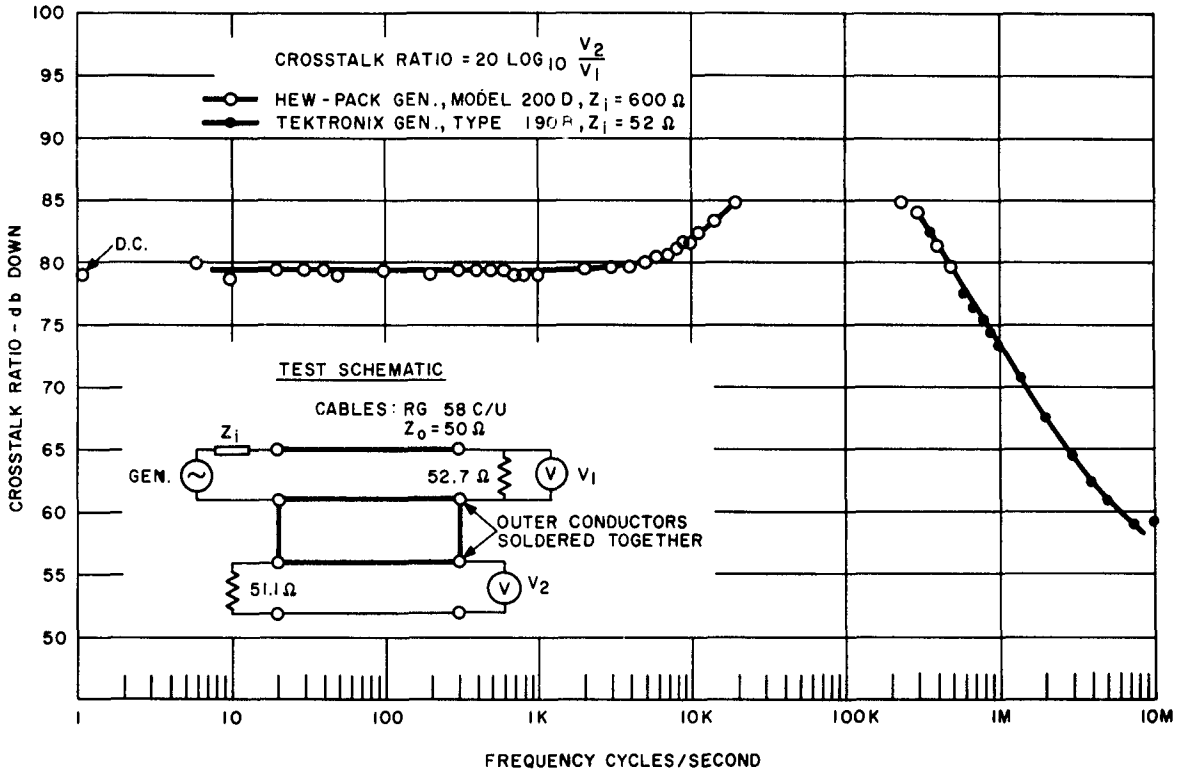


Figure 3-18. Extended Measured Crosstalk Between Cables

During the next quarter, a test set up will be constructed to measure the crosstalk ratios of miniature coaxial cable at frequencies from 0 to 10 kmc. This set up will compare the crosstalk ratio of ideally terminated cables to that of cables terminated as they will be on the presently proposed circuit wafers.

I. CALCULATED PULSE RESPONSE OF MISMATCHED CABLE

Information was desired concerning the reflected and transmitted waveforms due to various mismatched terminations of a transmission line. The form of pulse considered as a generating function is shown in Figure 3-20. The risetime of this pulse is short compared to the total period. It has the generally essential features such as risetime, fall time and a plateau; it is unsymmetric and conforms to the shapes of pulses encountered in computer technology.

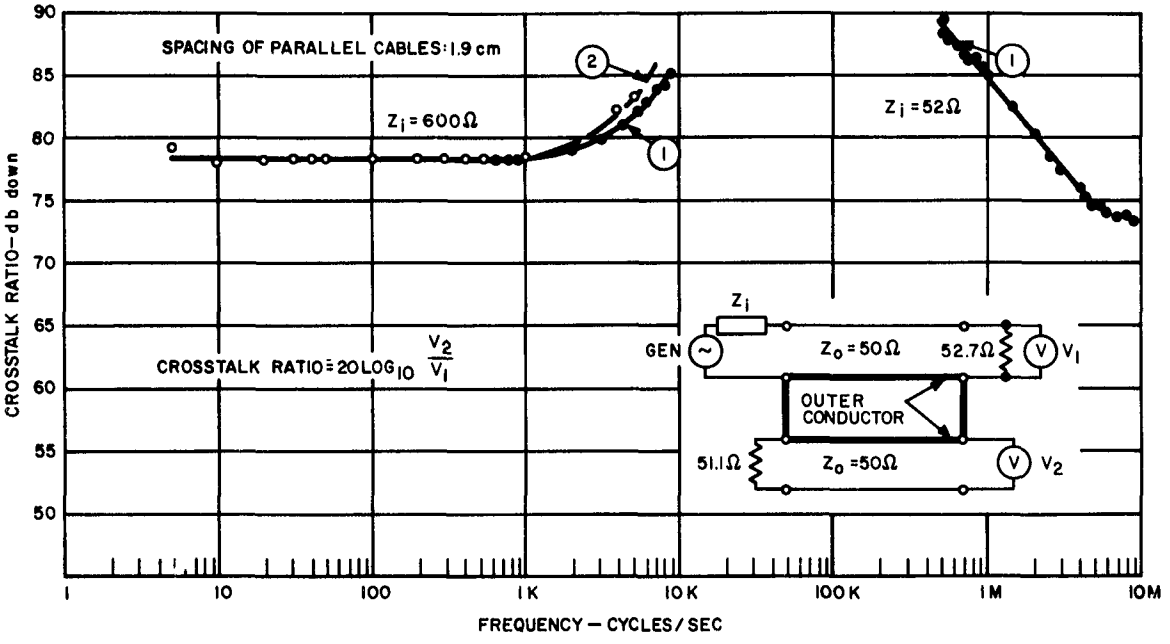


Figure 3-19. Measured Crosstalk with Improved Terminal Shielding

Using the pulse of Figure 3-20 as a limit function, the input waveform was synthesized by both a Fourier sum and Cesaro sum. This method was preferred over other methods because of its simplicity and straightforwardness. Some other methods are Laplace transform, solution of simultaneous differential equation, and the finite difference.

Of the two sums, the Fourier sum gives better approximation of the risetime of the limit function but this sum has a greater ripple. The Cesaro sum, on the other hand, synthesizes the input waveform more closely to that observed in the laboratory, but the risetime as well as the amplitude is more distorted.

The synthesized input waveforms by Fourier sum and Cesaro sum are shown in Figure 3-21 and 3-22, respectively.

As a preliminary test, the network of Figure 3-23 was considered as a termination of a lossless transmission line of 50-ohm characteristic impedance, the input end of which is matched to the generator.

The outputs due to the Fourier sum for different periods of repetition of the pulses are shown in Figure 3-24. The corresponding reflected waves are shown in Figure 3-25. For the component values considered in the terminal load, the reflected wave amplitude is almost equal to 98% of the incident waves are shown in

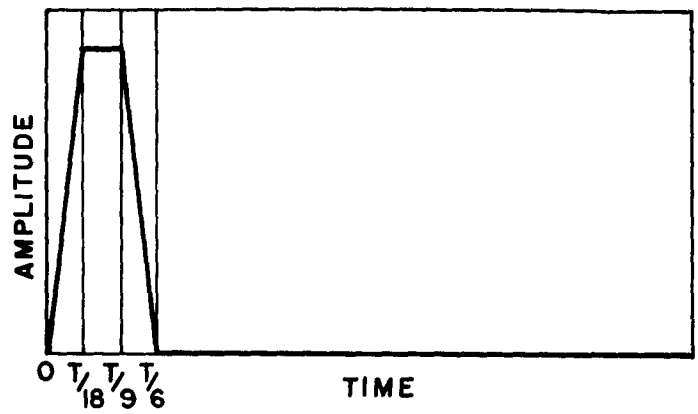


Figure 3-20. Generating Function for Pulse

period. The incident wave is half the input wave when the generator impedance is the same as that of the transmission line. A similar set of computations by Cesaro sum is underway.

Since the test problem gave a satisfactory result, a comprehensive study of the system is undertaken with the idea that the sets of curves that would result from the computation could be used as reference for other networks and pulses of different risetime.

An experimental set up is also under consideration to confirm the computed results.

J. COMPONENT TRIMMING

It has become apparent that tolerances are the most severe problem to be overcome in the design of tunnel diode circuits. A number of circuits have been designed which can operate, provided power supplies, circuit resistors and/or tunnel diode peak currents are adjusted. On the other hand, if economically obtainable tolerances are allowed for every component and for the power supplies, then operation under worst-case conditions becomes questionable at best for most circuits, and for many circuits impossible to guarantee.

The fact that by adjusting the power supplies most circuits can be made to function properly, suggests one possibility of overcoming the tolerance problems. The power supplies could be set at their normal values and the bias resistors adjusted until the circuit triggers properly with the worst-case inputs. Similarly, adjustable resistors can be used in interstage coupling and in gate-to-gate coupling branches to compensate for characteristic variations of coupling rectifiers.

In practice, adjustment of resistors is limited to an increasing direction only. This means that the circuits should be built with resistors which are below the nominal value, and then increased until the circuit reaches proper operation.

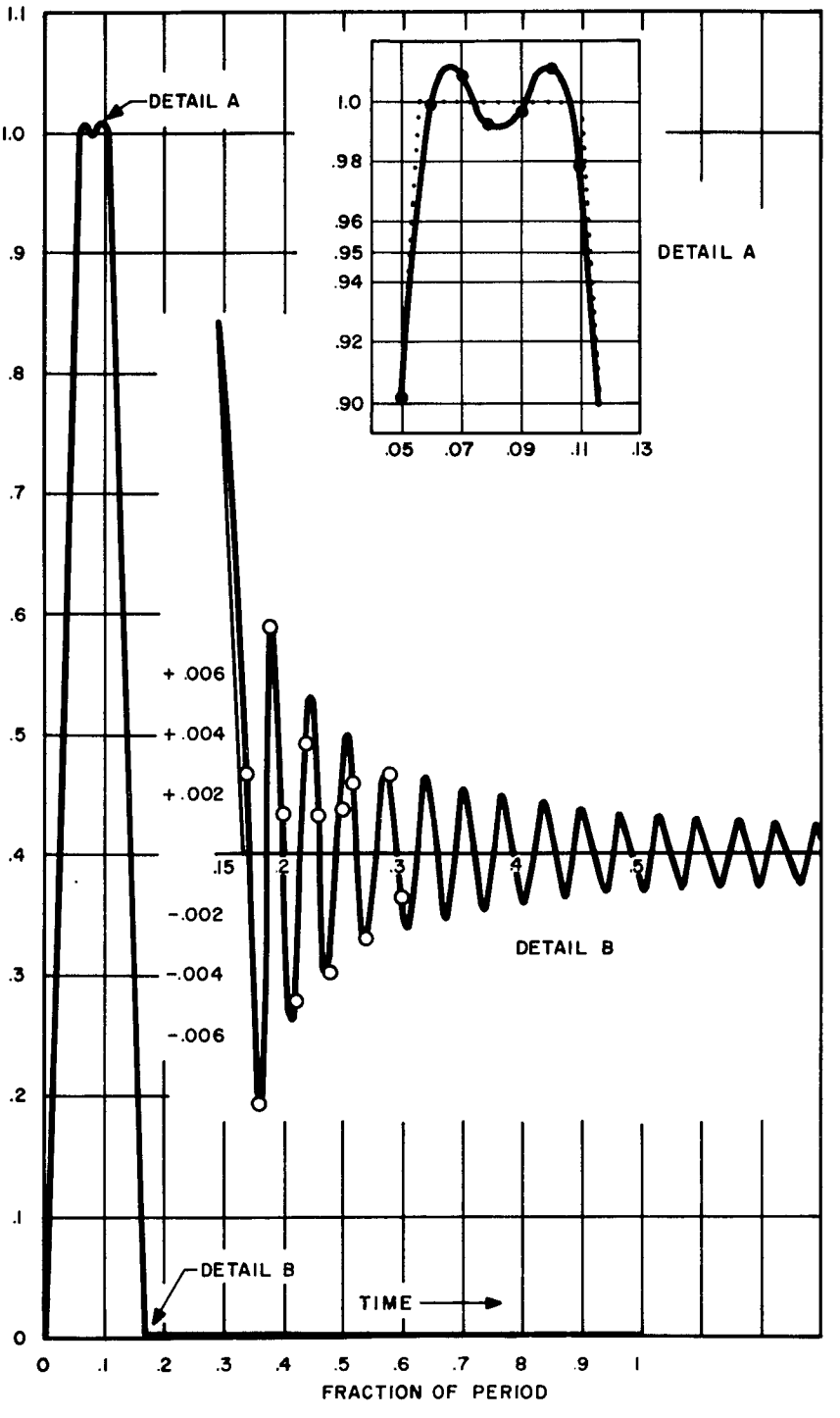


Figure 3-21. Input Pulse Using Fourier Sum

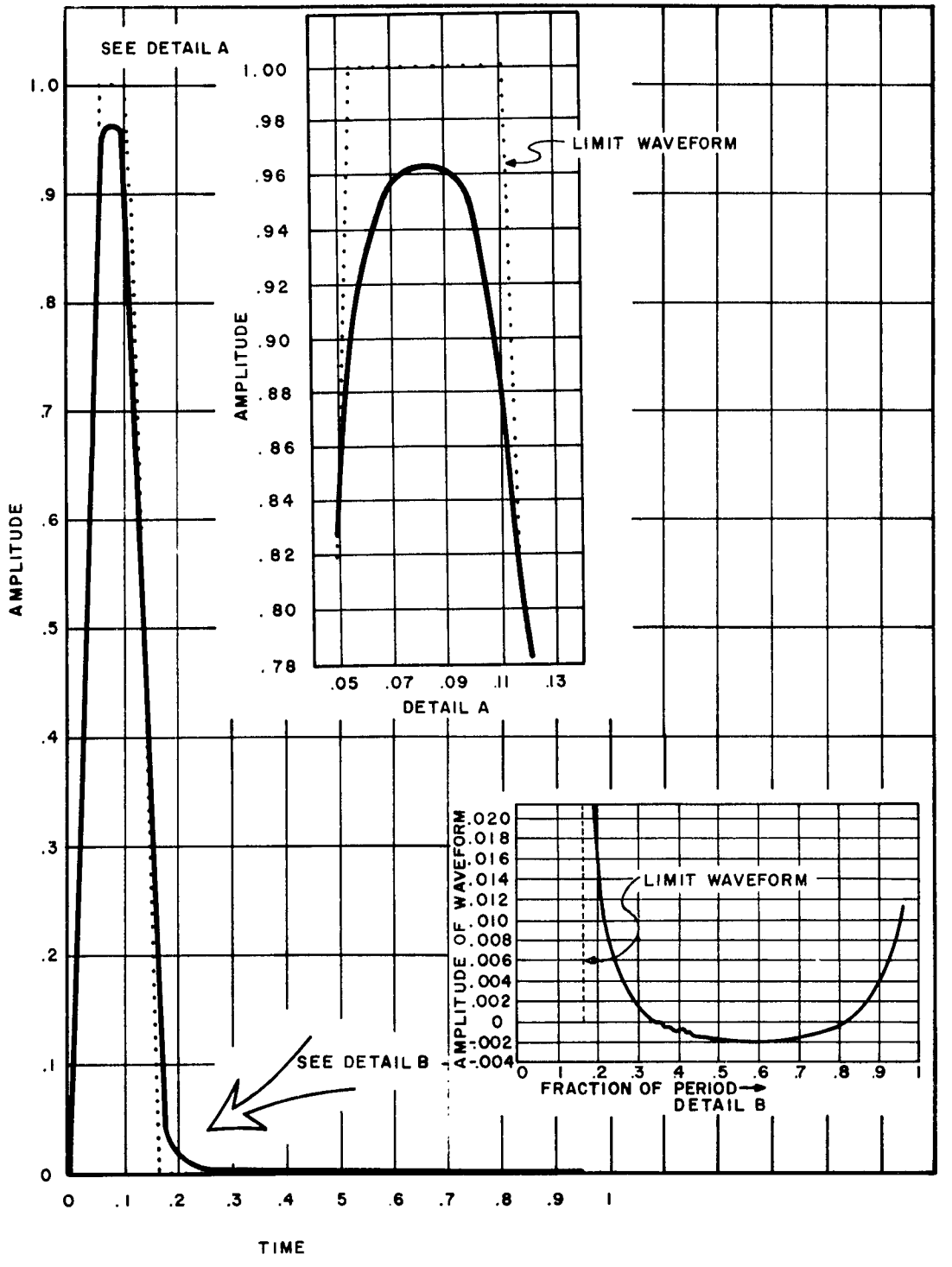


Figure 3-22. Input Pulse Using Cesaro Sum

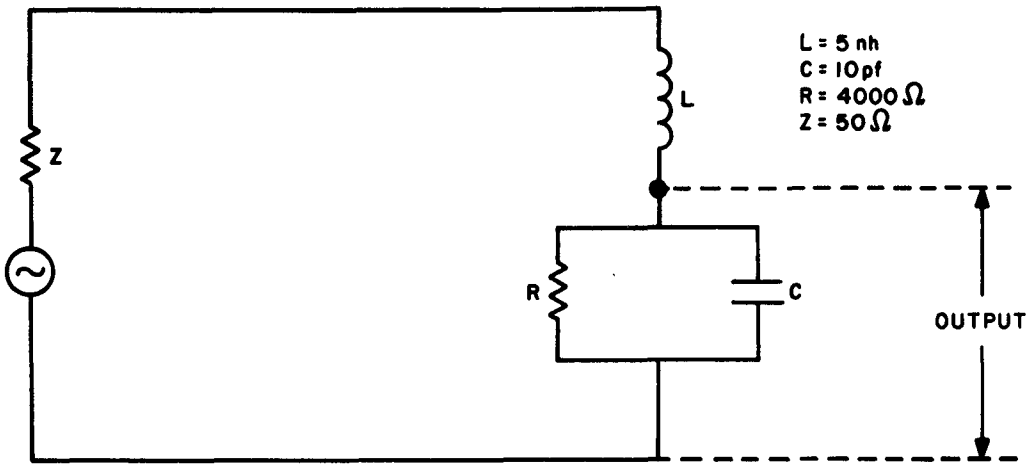


Figure 3-23. Terminating Network for Pulse Computation

1. Aims and Advantages

   (a) Aims - To show that the idea of adjusting (trimming) resistors is practical, develop practical techniques, and construct and operate "trimmed" circuit modules.

   (b) Advantages - These are as follows:

      (1) Gain and/or circuit safety factors will increase.

      (2) Gives the effect of closer tolerancing than is economically possible by specifying precision components.

      (3) Permits wider tolerances of diode characteristics.

      (4) Small changes in diode and resistor characteristics due to soldering can be compensated.

The advantages enumerated above can be better appreciated by considering the tolerance problem illustrated in Figure 3-26 (note that trimming will eliminate manufacturing tolerances of resistors and tunnel diode I_p) and also by referring to the circuits in Figure 3-27 and 3-27a.

Figure 3-27 is of a two-stage monostable OR gate, where no trimming is employed. The circuit shows the available and required currents at every significant point. The input and output tunnel diodes have peak currents of 24 and 48 ma, respectively. The results when trimming is employed is shown in Figure 3-27a. Note that the input current is now 4.7 ma instead of 7 ma, and the interstage current drops from 14 to 11.5 ma. Also, the fan-out increases from 3 to 4. Because the interstage current is reduced, the input stage peak current can be reduced from 24 to 20 ma.

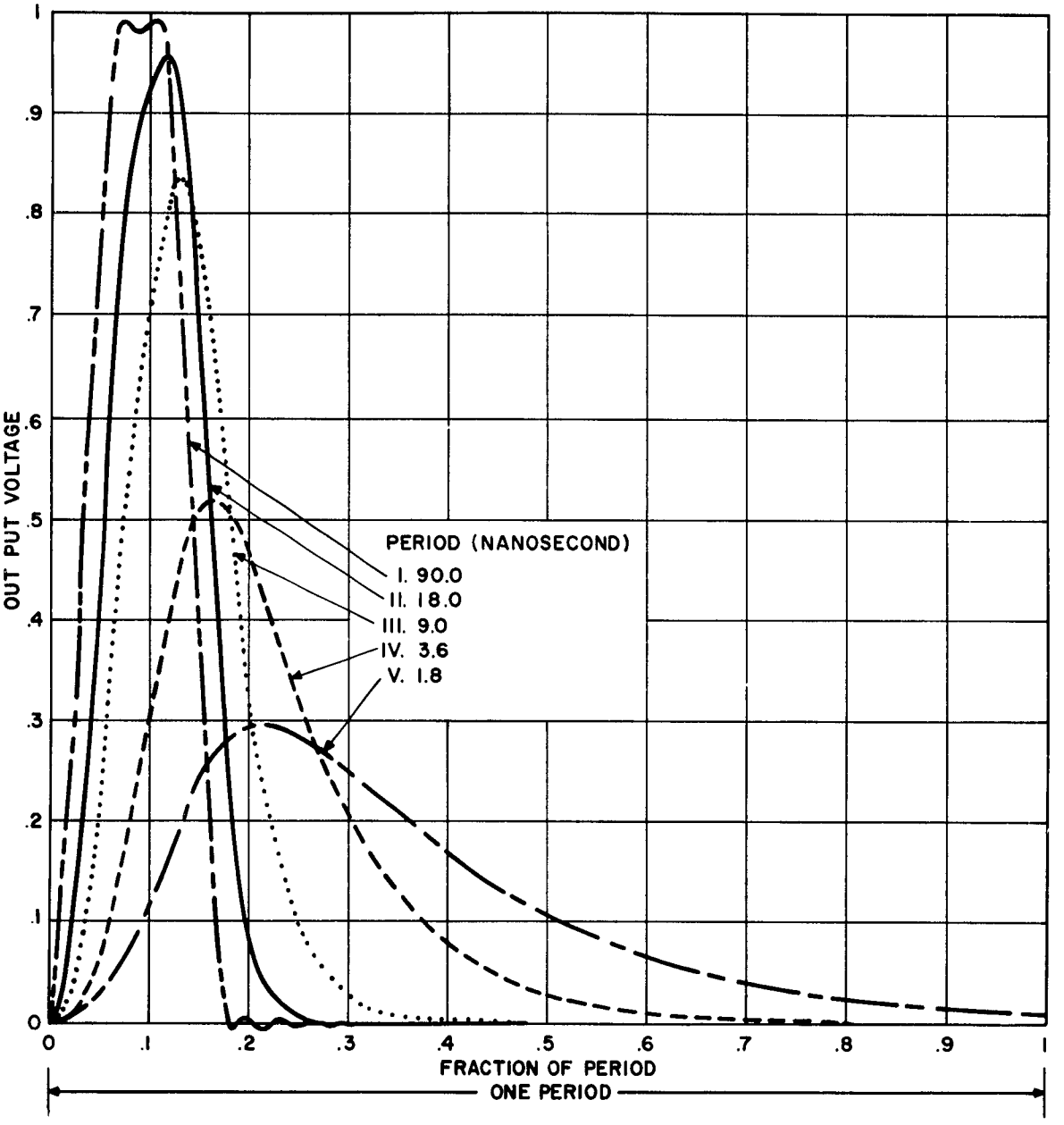


Figure 3-24. Output Waveforms of Mismatched Coaxial Cable

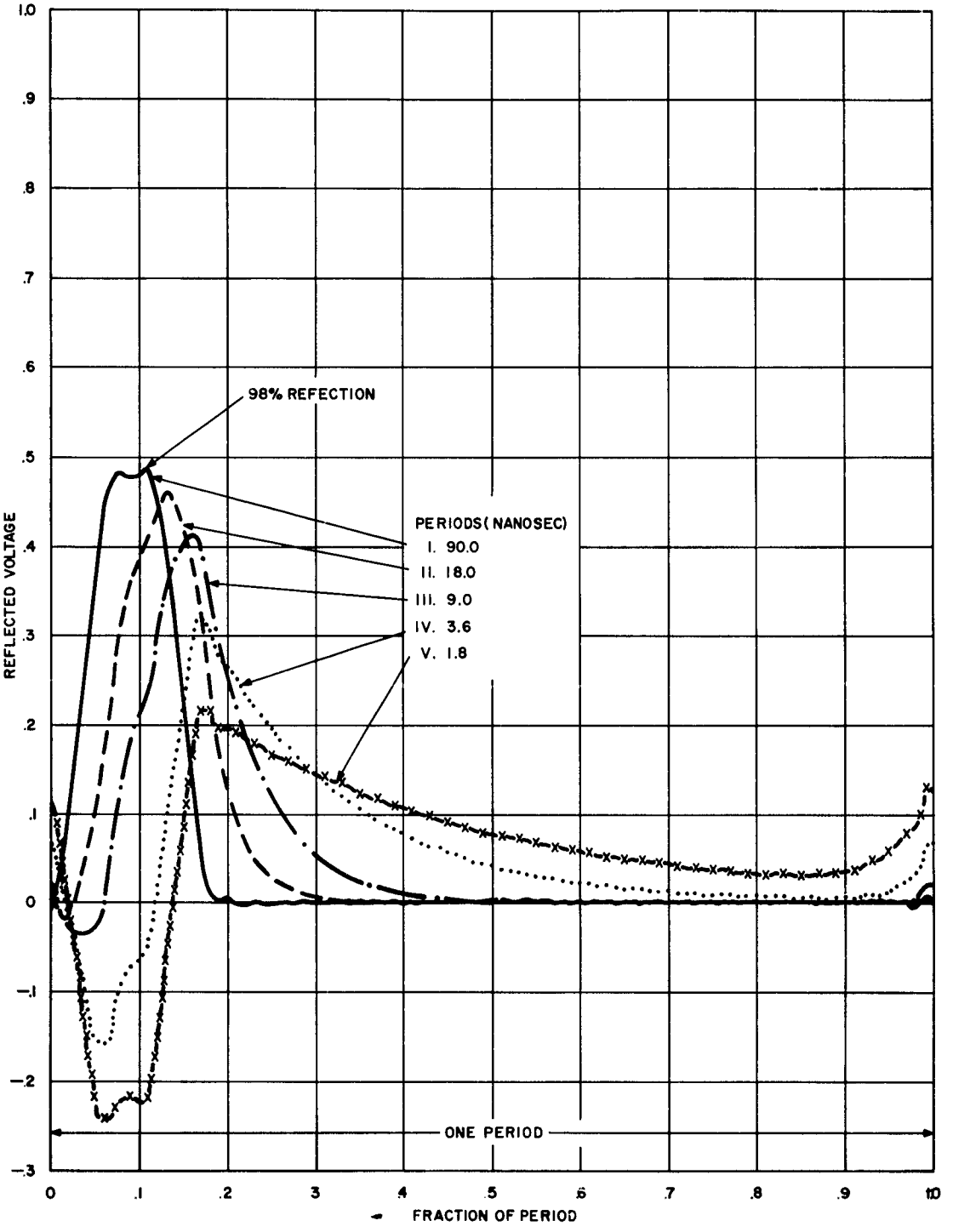


Figure 3-25. Reflected Waveforms of Mismatched Coaxial Cable

The various currents shown in Figures 3-27 and 3-27a were derived from the following expressions for bias current (I_B) and minimum switching current (I_{in}):

Untrimmed Case

$$I_B = I_p - I_p \left[\Delta I_{p(m)} + \Delta I_{p(A)} + \Delta I_{B(RM)} + \Delta I_{B(RM)} + \Delta I_{B(V)} + S\right]$$

$$I_{in} = I_p \left[2\Delta I_{B(V)} + 2\Delta I_{B(RM)} + 2\Delta I_{p(RA)} + 2\Delta I_{p(M)} + 2\Delta I_{p(A)} + S + X + L\right]$$

Trimmed Case

$$I_B = I_p - I_p \left[\Delta I_{p(A)} + \Delta I_{B(RA)} + \Delta I_{B(V)} + S\right]$$

$$I_{in} = I_p \left[2\Delta I_{B(V)} + 2\Delta I_{B(RM)} + 2\Delta I_{p(H)} + S + X + L\right]$$

The terms in these equations are defined as follows:

I_{in} = minimum input current

I_p = peak current

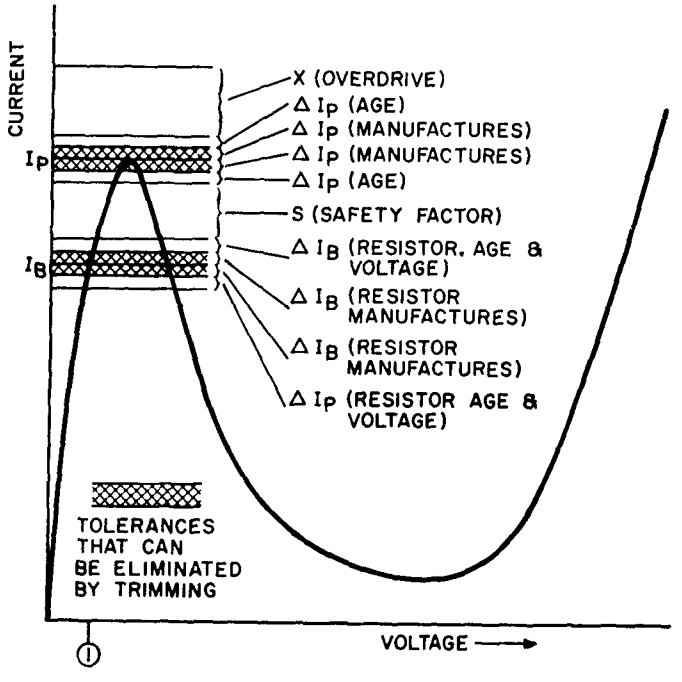


Figure 3-26. Tolerances That can be Eliminated by Trimming

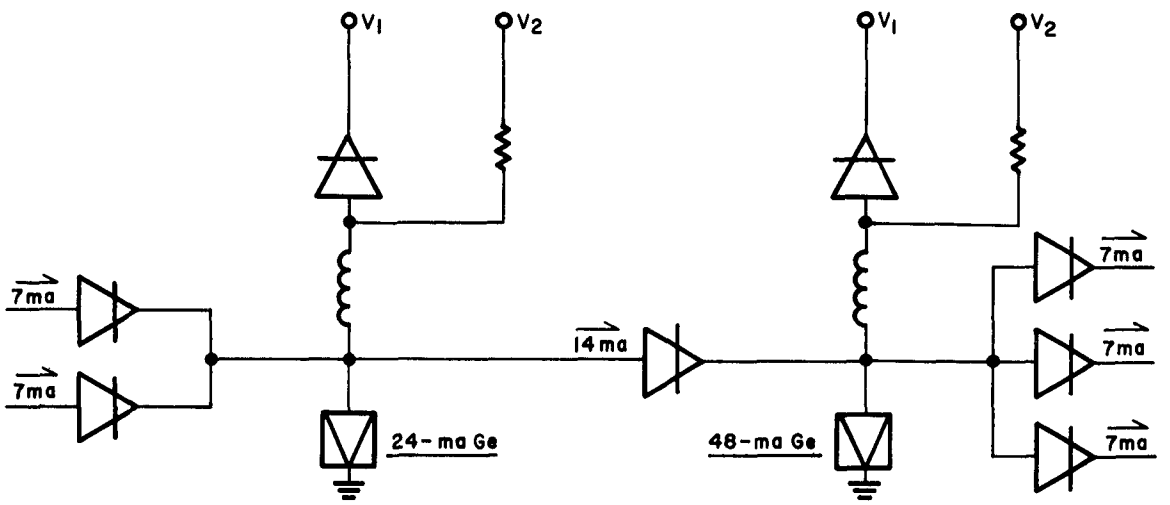


Figure 3-27. Untrimmed Wafer (Nominal Tolerances)

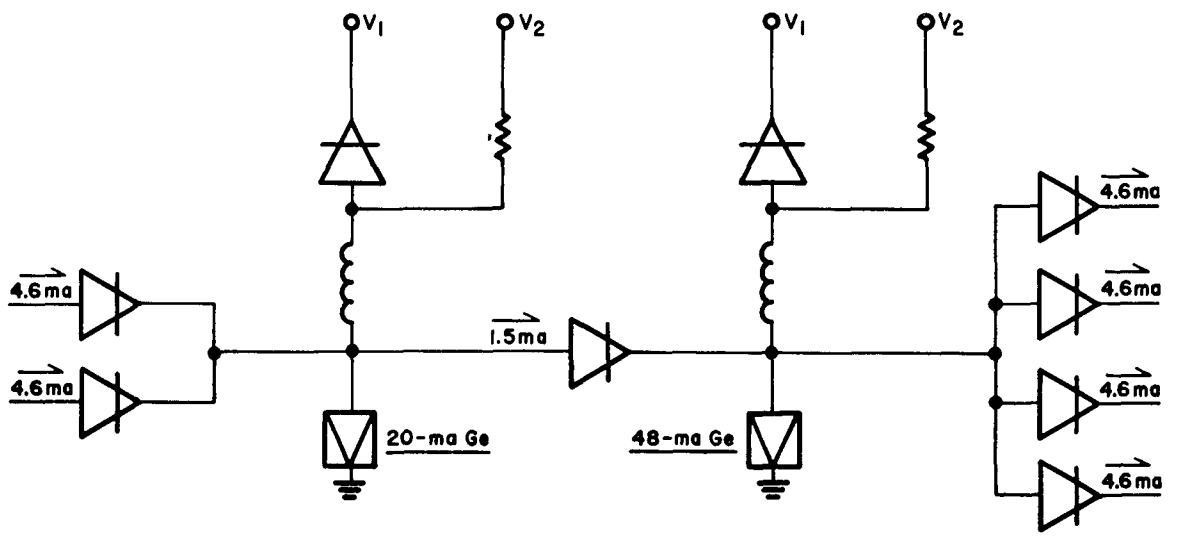


Figure 3-27a. Trimmed and Optimized Wafer

$\Delta I_{B(V)}$ = tolerance in bias current due to variations in voltage

$\Delta I_{B(RM)}$ = tolerance factor in bias current due to variations in the manufacturing tolerance of resistors

$\Delta I_{B(RA)}$ = tolerance factor in bias current due to variations in resistor because of aging.

$\Delta I_{p(M)}$ = tolerance factor in the peak current due to variations in the manufacturing tolerance of the tunnel diode.

$\Delta I_{p(A)}$ = tolerance factor in peak current due to variations in the aging of the tunnel diode

S = a current to represent a safety factor against noise

X = current to give a specific overdrive

L = current loss into load

The tolerances assumed to arrive at the currents given in Figures 3-27 and 3-27a are as follows:

	Tolerance
Resistor (Manufacturing)	±1%
Resistor (Aging)	±1%
Power Supply Variation	±2%
Tunnel Diode (Manufacturing)	±1%
Tunnel Diode (Aging)	1%
Safety Factor for Noise	±5%
Overdrive and Current Loss into Load	±10%

2. Trimming Method

In principle, resistors can be trimmed by scraping their surface with a hard object. Experiments conducted on several types of carbon and metal film resistors showed that a glass fiber brush or an abrasive blasting machine will do an adequate job. Thus, it is proposed that the circuits be assembled with resistors having values smaller than required for proper operation; then by brushing or blasting, the resistors can be brought to their proper value.

3. Implementation of Circuit Trimming

To implement the trimming technique, a set of standard loads and standard pulse and level generators are required. The number of standard loads required will depend on the fan-out of the circuit being trimmed, while the number of standard pulse generators will depend on fan-in.

Each standard load will consist of a tunnel diode circuit having a similar input impedance to that of the circuit being trimmed. Similarly, the standard input pulses and level generators are tunnel diode circuits having outputs which can be set to certain specified levels.

A circuit will be considered to have been properly trimmed when with the supply voltages and input levels and pulses set at their worst-case level, it will drive the specified number of standard loads. The procedure for trimming will be as follows:

(1) Connect the standard loads to the circuit to be trimmed.

(2) Set the power supplies for the final stage of the circuit. *

(3) The power supplies for the other stages will be set so that the current through each stage tunnel diode is just below the peak. (The final stage will now be generating pulses without a pulse input).

(4) Trim the bias resistor for the final stage by abrading surface until the stage ceases to generate pulses.

(5) Adjust the trimmed stage power supplies to the nominal voltages attainable by the power supplies.

(6) Set the voltages on the next stage to the same value as in step (2). (This stage will now be generating pulses. Similarly the final stage will generate a pulse for every pulse of the free running stage.)

(7) Trim the bias resistor for this stage until it stops generating pulses.

(8) Adjust power supplies as in step (6).

(9) Repeat in succession steps (6) through (8) for every stage until the input stage is reached. (For most circuits, the maximum number of stages is three: an input stage, an amplifying stage, and an output stage.)

(10) Adjust the power supplies for the input stage to their minimum design value.

(11) Set the level input from standard level generator to minimum standard level.

*The 6-volt supply is set to its maximum value, the 100-mv supply is set to its minimum.

TABLE 3-5
EFFECTS OF TRIMMING ON CARBON FILM RESISTORS WITH STABILITY AS A FUNCTION OF TIME AND LOAD

Measured Under Load							
Res. No.	No Load Value	Trimmed Value	Value after 123 hours	Value after 334 hours	Change due to Trimming	Change due to aging	Load Condition
	(Ohms)	(Ohms)	(Ohms)	(Ohms)	(%)	(%)	(MW)
1	5.98	6.06	6.12	6.08	1.0	1.0	125
1	6.07	None	-	-	None	0.0	250
2	5.98	6.19	6.27	6.23	3..5	1.3	125
2	6.21	None	-	-	None	0.3	250
4	110.5	124.0	124.9	124.1	12.2	0.71	125
4	124.0	None	-	-	None	0.1	250
5	112.0	154. 0	153.6	152.8	37.5	0.0	125
5	153.0	None	-	-	None	0.0	250
7	157.0	162. 0	162.0	-	3.2	0.0	125
7	162.0	None	161.2	-	None	0.0	250
8	157.0	171.0	171.0	-	9.0	0.0	125
8	171.0	None	171.0	-	None	0.0	250

(12) Set standard input pulse 4.5% below minimum design value. (The output stage will now be generating an output pulse for every input pulse.)

(13) Trim the bias resistor until stage stops generating pulses.

(14) Increase standard input pulse 5%. (stage will now trigger)

(15) Check each of the outputs from the standard loads to insure that the output stage is delivering the minimum current into each standard load.

(a) If each load is firing, the trimming is completed.

(b) If all the loads are not firing, then the output stage coupling resistors must be trimmed to insure that the current from the output stage divides equally among the standard loads.

4. Present Status

The feasibility of the trimming technique described under paragraph 3 has been demonstrated on several single-stage, tunnel-diode gates. Samples of the following types of resistors are being tested.

(a) Carbon film (Pyrofilm, Inc.)

(b) Evaporated nichrome film (Film Resistor, Inc. and Filmohm)

(c) Evaporated precious metal film (American Components, Inc.)

A test set up consisting of standard loads and input generators is under construction. This set up will permit the trimming of AND gates, OR gates and bistable circuits.

Table 3-5 shows the results of tests of stability vs. load and trimming for samples of carbon film resistors by Pyrofilm, Inc. Work on other types is continuing.

III. PROGRAM FOR NEXT INTERVAL

Crosstalk in transmission lines and connectors will be measured. Electrical properties of 10-mil diameter coaxial cable will be studied. Obtainable tolerances on characteristic impedance for minature coaxial cable will be determined.

Optimum procedures for handling miniature film resistors will be determined. Pulse waveforms occurring on mismatched cable will be computed.

A circuit trimming bench set up using an air abrasive unit, suitable input circuits (to give standardized pulse and level outputs) and various loading circuits will be built. Two- and three-stage AND and OR circuits will be assembled and trimmed.

Two-stage AND gates having diodes with peak currents optimized for trimming will be designed, built, trimmed and tested.

Test and evaluation of resistors will continue.

Chapter 4. LOGIC SUBSYSTEM

SUMMARY

Significant changes have been made in wafer design and fabrication techniques to be used in the subsystem. Operation of a small group of logic circuits using these techniques has been accomplished.

Specifications for low-impedance power distribution lines have been finalized and samples are being tested.

The system concept of the logic subsystem remained essentially unchanged. The major modifications were caused by changes in logical circuit complement from a set-trigger bistable to a set-reset bistable. During this period, the control console was further defined to permit greater flexibility in operation and greater ease in maintenance of the logic subsystem. Several wafer placement layouts were made in an effort to minimize interconnection wiring delays.

Chapter 4. LOGIC SUBSYSTEM

I. PERSONNEL

The following personnel contributed to this phase of the project during the eleventh quarter:

A. R. Alter
F. Borgini
J. W. Harmon
R. E. Herr
D. H. Hull
R. J. Linhardt
J. P. McAllister
J. L. Miller
H. V. Rangachar
D. E. Roop
M. A. Schrader

II. DISCUSSION

A. WAFER DESIGN

During this quarter the placement of the logic circuits on wafers underwent a major redesign. The wafer size was progressively increased from a width of .775 inch to 1.2 inches and finally to 1.5 inches. The height of the final wafer design is .7 inch for the bistable and monostable AND gate, and .6 inch for the monostable OR gate. The final design considerations included both fabrication and electrical limitations.

By increasing the width to 1.5 inches, it is possible to place the entire bistable circuit on a single wafer. This size also makes it possible to place the three-stage AND circuit on this wafer. A photograph of this wafer before and after assembly can be seen in Figure 4-1. As with the smaller wafer, all signal connections will be made on the base of the wafer with all power connections made on the sides. The circuit layout on the wafer was based on minimum path length and the ability to monitor circuit operation by strategically placed test points at the top of the wafer. The wafer size and approximate transmission path length is given in Table 4-1.

TABLE 4-1
WAFER SIZE AND TRANSMISSION DELAY

Function	Wafer Size (inches)	Transmission Path (inches)	Approximate Transmission Delay (ns)
AND	.7 x 1.5	2.75	.34
OR	.6 x 1.5	1.95	.24
BISTABLE SET	.7 x 1.5	2.25	.28
BISTABLE RESET	.7 x 1.5	2.45	.31
DELAY	.7 x 1.5	2.6	.33
LOAD	.6 x 1.5	----	---

At the present time, construction has just begun using the 1.5-inch, final-size wafer. Seven OR circuits as well as five bistable circuits were built and tested using the 1.2-inch wafer size.

It was decided during this quarter to use teflon for the wafer construction. This decision was made on the basis of its ease of fabrication and low dielectric constant as compared with ceramic. Electrically, since the dielectric constant of teflon is 2.4 and that of ceramic is approximately 6 in the worst case, the path delay on ceramic should prove to be 1.57 times that of teflon. As shown in Figure 4-2, this ratio was confirmed in the laboratory by measuring the delay through identical .700 x .775-inch blank wafers with a path length of 1.75 inches. The absolute observed delays proved to be somewhat greater than those calculated; however, the calculations were based on a distributed line theory whereas the wafer path appears to be a lumped constant line of variable magnitude. The ceramic wafer output is somewhat distorted, as seen in the figure, due to difficulty in obtaining a good impedance match at the input and output. Laboratory tests were made on completely assembled .700 x .775-inch ceramic and teflon OR wafers. The teflon wafer proved to have .5 ns shorter transit time than the ceramic. It should be noted that considerable care was taken to assure that the measurements were taken under identical electrical conditions. Transit time measurements were also made on three, 1.2 x .6-inch teflon OR wafers and found to be 1 ns. Path delay was also measured on these wafers as being .45 ns leaving a switching time of .55 ns which agrees quite closely with the time calculated by the Logic Circuits Group.

B. WAFER CONSTRUCTION

Several problems in wafer construction have been encountered; solutions to these were developed during this quarter.

1. Tunneling Devices Failing

Considerable attention was focused on this situation with the result that this problem seems to have been solved. At the beginning of the quarter as high as 30% of these devices were being damaged during the assembly operation. This was corrected through the use of a screen rather than a tab assembly and the use of 5-mil Kovar in place of 2-mil Kovar in the package. The package tabs are now being bent, cut, and tinned to minimize handling during assembly. These device improvements, coupled with improved soldering techniques, have made the assembly of diodes a relatively reliable operation.

2. Filter Capacitor (barium-titanate inserts on wafer frames)

The plating on these capacitors lifted during soldering. This problem was resolved by changing the process by which the silver pattern is applied to the ceramic and by improved soldering techniques.

3. Resistors Changing Value

Improvement was gained in this area by pre-tinning the resistors. Further investigation of this problem will continue during the next quarter.

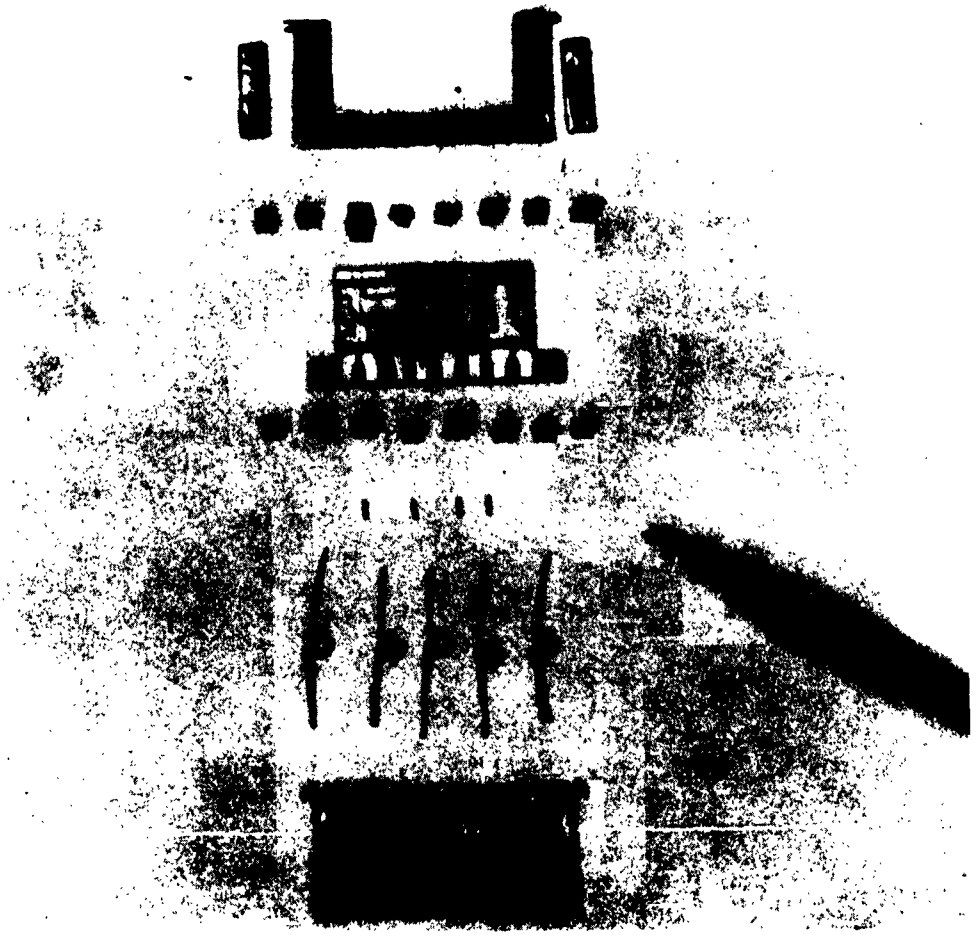


Figure 4-1. Bistable Wafer Construction

.5 NANOSECOND/DIV

Figure 4-2. Output from Blank Teflon and Ceramic Wafers vs. Input

C. WAFER TESTING

The wafer test fixture (Figure 4-3) presently in use is an adaptation of one previously constructed for .700 x 775-inch wafers. The power supplies are connected to the fixture by low-inductance coaxial lines and on the fixture itself the wafers are supplied from low-impedance lines of the type to be used in the subsystem. Connections to the wafer filter capacitor are made by bridge-spring contacts. The necessary signals are brought into the fixture on standard coaxial lines from a signal generator and then carried to the wafer by miniature coaxial lines of the type to be used in the subsystem. These lines are attached to spring contacts at their terminals. This arrangement enables rapid testing of the wafers since they can be inserted and removed easily. Wafer operation can be tested at each point in the circuit since all points are accessible during circuit operation. From measurements made with this test fixture, in conjunction with the Tektronix curve tracer, deviations from design specifications can be determined and readily corrected.

Pictures of waveforms obtained using the wafer test fixture are shown in Figures 4-4 and 4-5. These waveforms were obtained at one of the test connectors through a coaxial cable making spring contact with one of the wafer output tabs. The output of a typical monostable circuit and that of a typical bistable circuit are shown in Figures 4-4 and 4-5, respectively. These waveforms agree quite well with those predicted by the analysis made of a mathematical model using a digital computer.

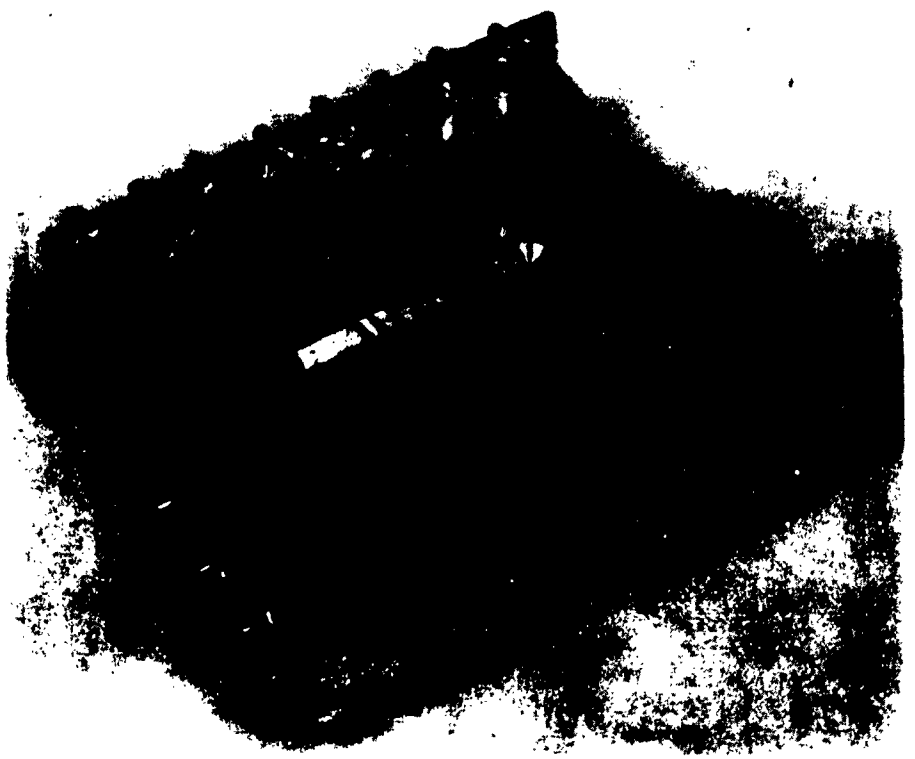


Figure 4-3. Wafer Test Fixture

In testing the 1.2-inch wafers, the chief causes of wafer failure were found to be resistor variation and faulty filter capacitors. Resistors were found to vary by as much as 10% from nominal values where circuit design specifications call for 1% tolerance. A study of this problem is being conducted. Improved material and soldering techniques, now being investigated, should relieve the filter capacitor problem.

D. CIRCUIT EVALUATION

The first phase of integration of teflon wafers with open frame assembly resulted in the operation of five monostable circuits at a repetition rate of 150 mc. The logic diagram of these circuits is shown in Figure 4-6. These wafers were operated under conditions which will be used in the subsystem; that is, using low-impedance power distribution and miniature coaxial signal connections. Also, the wafers were pretested before assembly for proper operation under specified conditions, as will be done prior to incorporating them into the subsystem. The wafer size used was 1.2 inches, with AND gates consisting of two-stage OR gates biased such that two inputs were required for switching. These wafers were connected in the configuration shown in Figure 4-7.

The input to the first OR gate is 300-mv pulses at a 150-mc repetition rate; the output of this gate in turn drives two AND gates. Operation of the AND gate was then accomplished by the application of a 160-mv d-c level to the second input. The output of these two circuits in turn triggered two more OR gates. The outputs of the two OR gates were approximately 300 mv each, as seen in Figure 4-8. The slight difference in the two outputs was probably due to a slight difference in the inductance of each wafer.

The signal wiring used was 30-ohm coaxial cable formed by drawing a copper shield over teflon insulated wire. The outer shield of these cables was soldered to the wafer holders, with the inner conductor soldered to appropriate tabs on the wafer.

Delays were measured through the two paths which included the delay through wafers and signal wiring. The delay through each path was approximately 4 ns. At present this frame is under life test and at the time of this writing has been in operation for 144 hours.

A three-stage AND wafer, illustrated in Figure 4-9, was checked this quarter. This wafer was driven by two OR gates, one simulating an operating bistable and the other providing the pulse input. The transit time for this AND gate was 2 ns as seen in Figure 4-10.

E. LOW-IMPEDANCE POWER DISTRIBUTION

Work on the low-impedance power distribution system has continued essentially on the lines planned at the end of the last quarter. A new design for the lines has been worked out to suit the new logic circuits which will be used in the subsystem. These lines have been specified and drawings have been prepared for the convenience of the vendors who are willing to undertake the manufacture of this item. Tests have been conducted to study the electrical characteristics of the lines, and to determine

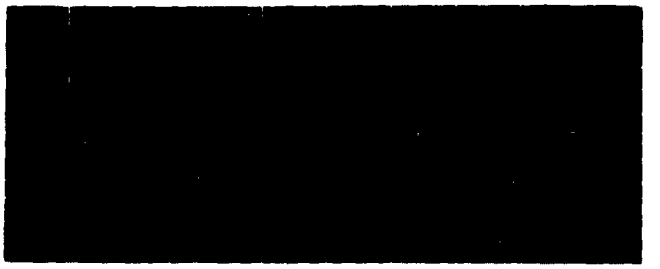


Figure 4-4. Monostable Waveform — Using Wafer Test Fixture

Figure 4-5. Bistable Waveform — Using Wafer Test Fixture

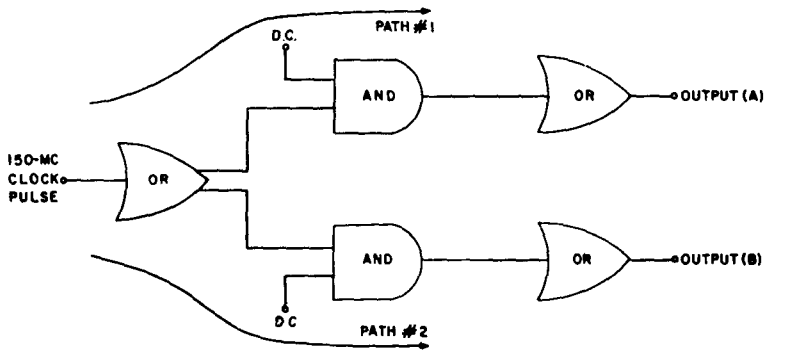


Figure 4-6. Logic Diagram Showing Operation of Wafers in Frame and Associated Signal Paths

Figure 4-7. Wafer Frame Assembly

the effect of unterminated lines. A fabrication technique has been developed so that these lines can be built in our laboratory in case no vendor can supply them to our satisfaction. Wafers have been made to satisfactorily operate from these lines in the laboratory.

1. New Power Distribution Design

The new logic circuits require three voltages: +100 mv, +6 volts and -6 volts. The monostable stages need only the +6-volt supply and the +100-mv supply, with only the bistable stages needing all three supplies. The waveform of the current changes that occur at the various supply points have been furnished by the circuit design group. The monostable stages create a triangular current change at the current source and the clamp source, as shown in Figure 4-11. For this the worst case is assumed to occur when all the stages on a wafer begin to act simultaneously at a given instant and to continue acting thereafter at a repetition frequency determined by the base width of the triangle. This waveform is then analyzed into its components which comprise a step function, a fundamental and its harmonics. The characteristic impedance of the low-impedance lines are calculated from the magnitude of the step function amplitude, in accordance with the procedure set forth in IRR-9A. In the case of the bistable circuit, only the output stage creates a step-function current change at the current source. The magnitude of this step function is much smaller than that created by the monostable circuits. Thus, the impedance of the distribution lines have been determined mainly by the monostable requirements.

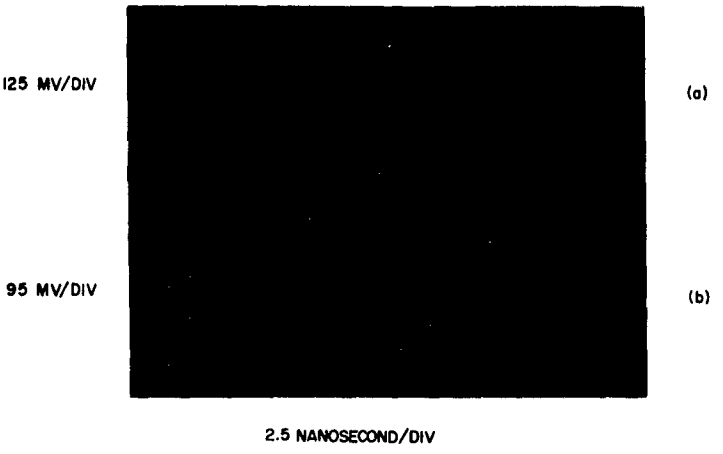


Figure 4-8. Switching Waveform — Five Circuits in Frame

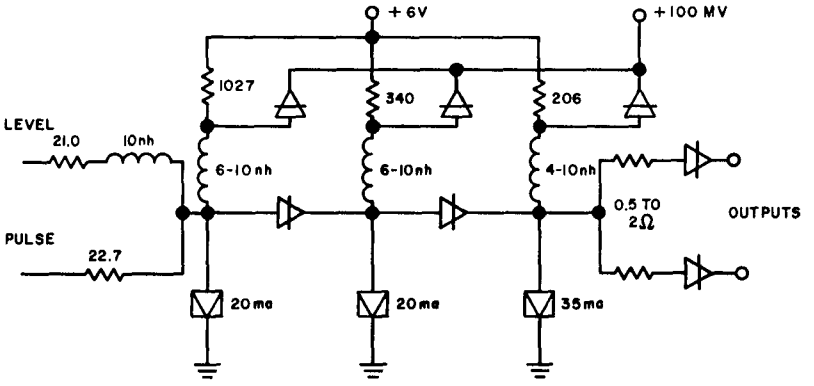


Figure 4-9. Three-Stage AND Gate

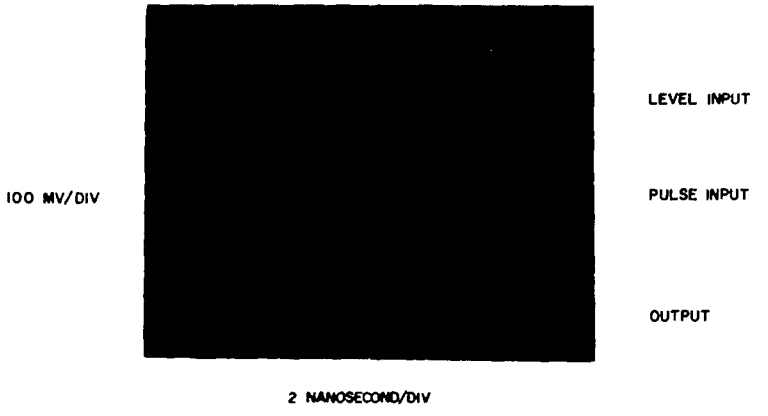


Figure 4-10. Input and Output Waveforms for Three-Stage AND Gate

The characteristic impedance for the 100-mv line is calculated to be 310 milliohms and for the +6v and -6v lines 7 ohms; but due to fabrication convenience, all three lines are proposed to be built on the same piece of ceramic material. Thus, the dimensions of the +6v and +6v lines were decided upon mainly for ease in fabrication, mechanical strength and d-c current carrying capacity. Because the -6 volt supply is needed only for the bistable circuits and only one side of wafers carrying the bistable circuits, the -6v line has been eliminated from the opposite side of the wafer. This available space has been utilized by widening the 100-mv line. This provided a lower impedance on the line which is very beneficial. Drawings and specifications, Nos. 8527829 and 8527838, have been prepared and vendors interested in supplying these items have been contacted. At present, preliminary samples from these vendors are being checked prior to the ordering of parts. The actual dimensions of the lines are shown in Figures 4-12 and 4-13.

a. Fabrication

In order to safeguard against the possibility that the vendors may be unable to supply acceptable samples, arrangements have been made to fabricate these lines in the laboratory. Ceramic pieces having dimensions which conform to those given in Figures 4-12 and 4-13, with the proper pattern silvered on thin surfaces, were purchased from Gulton Industries, Metuchen, N. J. These pieces are then copper plated in an electroplating tank and the copper is built up to 5-mils thickness. Then a strip of copper, 5-mils thick, with spot welded tabs is cut to widths corresponding to the widths of the different lines. These strips are then soldered to the lines on the ceramic pieces and the whole assembly is inserted into an I-beam by soldering in an oven. These I-beams, thus assembled with the low-impedance lines, will form part of the framework of the subassemblies in the subsystem.

b. Testing

Testing of the lines which have been built in the laboratory to determine risetime and characteristic impedance is continuing. The method used for testing is described in detail in IRR-10A. Further experiments on the same lines, but oriented to give information about the effect of mismatches at the end of the distribution lines, have been conducted. One of these was to build a frame made up of the distribution lines as shown in Figure 4-14, and to observe the propagation of pulses on such a frame. If the outside distribution ring was intimately joined to the feeder lines, the joint should act as a matched impedance only to the pulses leaving the feeder lines. A mismatch should be seen when these pulses try to re-enter the feeder lines, thus the ring can be used as a collector of the pulse disturbances. However, when the experiment was conducted, the joints were seen to introduce large discontinuities, which made the ends of the feeder lines appear as open circuits. Satisfactory right angle joints between distribution lines have proved to be a very difficult design problem, and to date, satisfactory answers have not been found.

Experiments were conducted to evaluate a series combination of a capacitor and resistor for termination. This scheme is shown in Figure 4-15. The resistor is 0.3 ohm which matches the line impedance. The capacitor chosen is large enough to give about 0.03 ohm impedance at 2 mc. The results of this experiment were

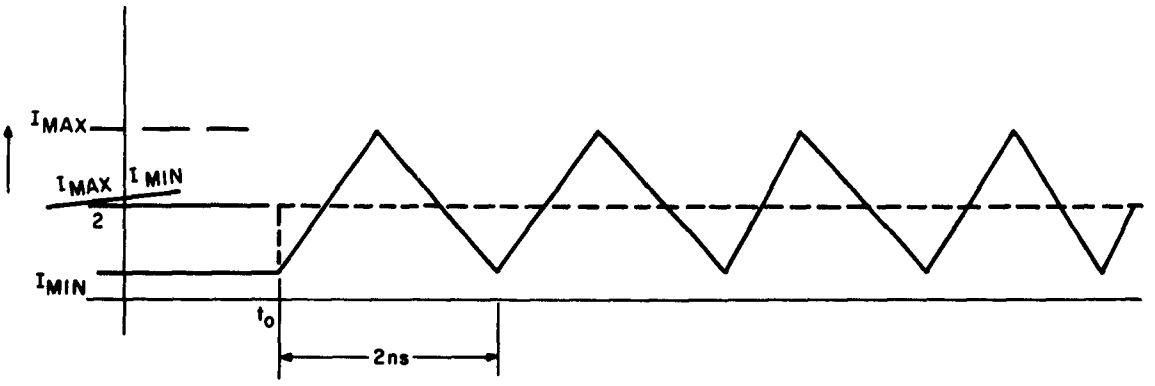


Figure 4-11. Disturbance of Monostable Logic Circuit

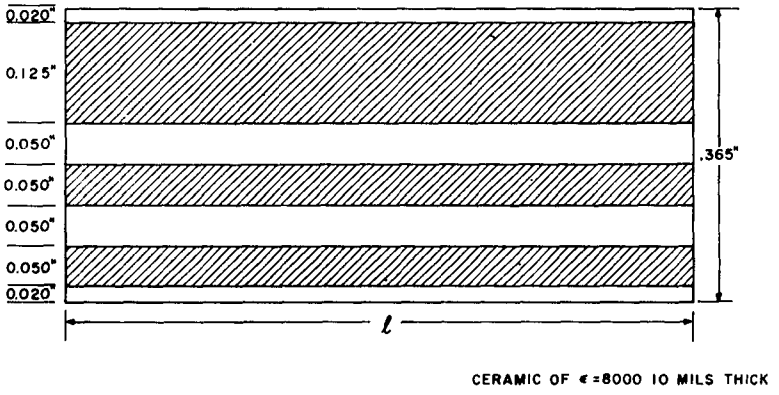


Figure 4-12. Details of Power Distribution Assembly — Type 1

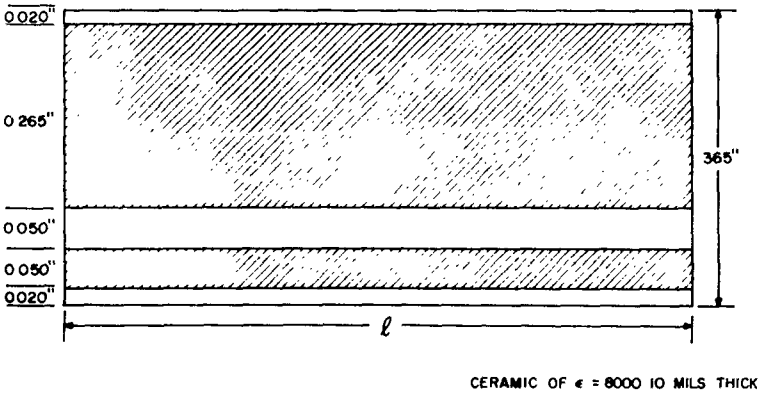


Figure 4-13. Details of Power Distribution Assembly — Type 2

Figure 4-14. Low-Impedance Distribution Frame

negative. The capacitor used was a 2.2 uf monolylic capacitor from the Sprague Co. This capacitor, combined with lead inductances (although they were cut down to the barest minimum) probably failed to give low impedances at the high frequencies of interest.

Another type of high-pass termination, the scatter method, has given encouraging results. In this scheme, Figure 4-16, the low-impedance supply line is branched out into a number of lines of higher impedance (i.e., smaller width) such that at the joint, the high-impedance lines present a match. The disturbances with energies predominantly in the high frequencies can enter the high-impedance branches, but cannot leave them to re-enter the low-impedance lines because of the severe mismatch in this direction. Thus, the pulse will eventually be attenuated by multiple reflection in the high-impedance branches. Preliminary trials using this scheme have confirmed its expected high-frequency attenuation properties. Details of the experimental line are given in Figure 4-17. Further work has been planned in this direction.

To determine the range of the terminating impedance which causes very small reflections, an experiment as illustrated in Figure 4-18 was conducted. The low-impedance line was terminated with a strip of silver paint (silver paint 200 Degussa, made in Frankfort, West Germany). The silver paint has a resistance of about 5K when fresh, and gradually decreases as it cures. When it is cured, it offers a resistance which is less than 100 milliohms.

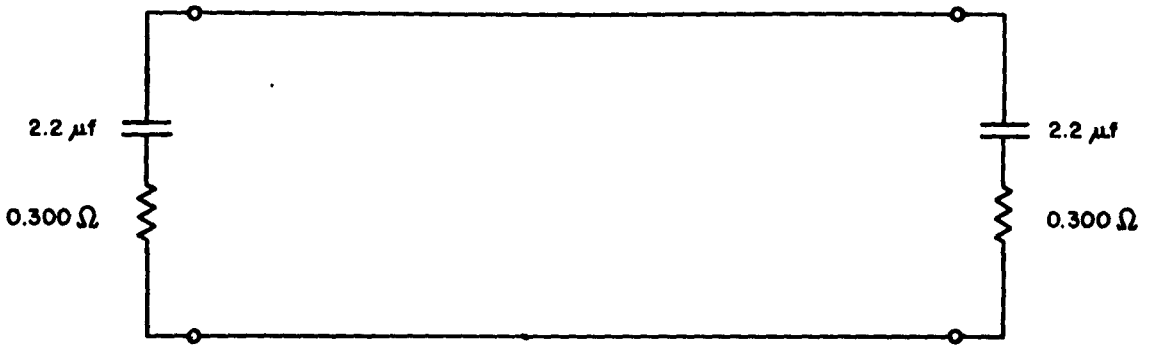


Figure 4-15. R-C Termination

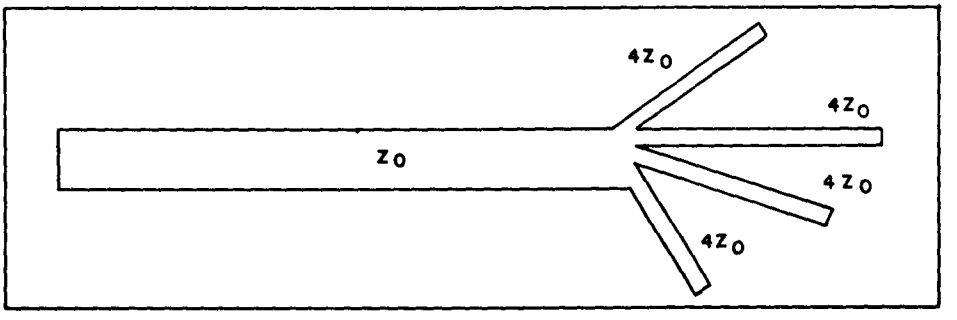


Figure 4-16. Proposed Termination Using Scatter Method

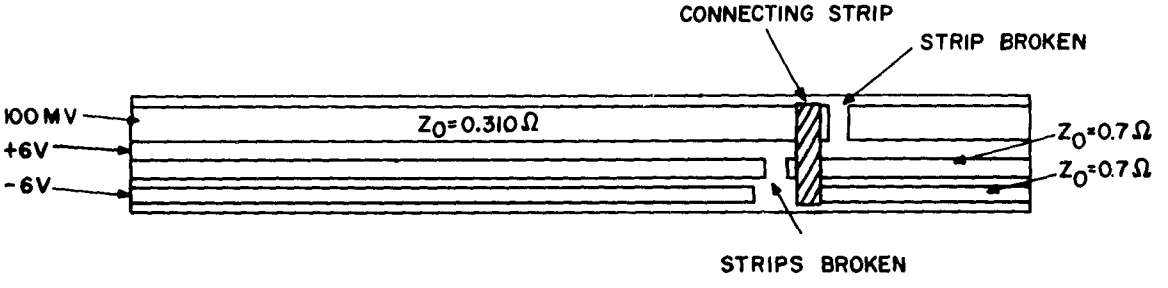


Figure 4-17. Details of Experimental Line which Confirmed Termination Using Scatter Method

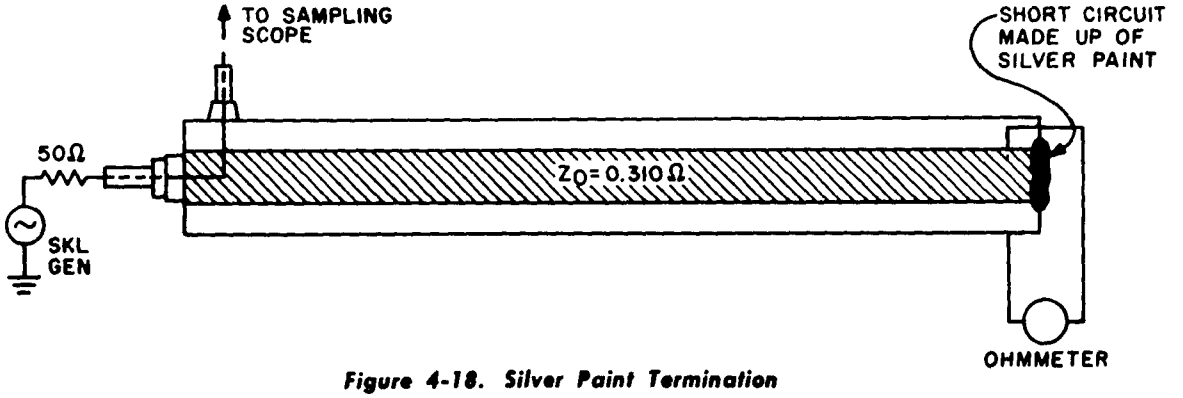


Figure 4-18. Silver Paint Termination

An ohmmeter was arranged to indicate this resistance and the line was pulsed with an SKL generator. It was observed that when the paint was "green" the reflections were like those obtained when the line was open. As the paint cured the reflections were observed to diminish in amplitude until, at a resistance reading of 0.310 ohm, no reflections were observed. After the resistance began to fall below 0.310 ohm, the reflections reversed in polarity and attained a large amplitude when the resistance value was indicating a short circuit. The reflections of small amplitude were observed for resistance values between 0.5 to 0.2 ohm, which corresponds to a reflection coefficient of ±0.25. This experiment indicated that the matching networks to be used must provide an impedance as low as 0.5 - 0.2 ohm in order to behave as an acceptable termination. It also represents an interesting and accurate method of measuring the characteristic impedance of a line.

The low-impedance lines have been designed using worst-case considerations which have, perhaps, improbable occurrence. Because of this, it may be possible to use the lines with no terminations. Experiments to investigate this possibility have been conducted and are reported elsewhere in this report. Calculations of the disturbance amplitudes that arise on the lines under actual operating conditions have been made. These have also been covered elsewhere in this report.

2. Frequency Response Tests

Several attempts were made to determine the attenuation in the line at various frequencies. Due to the low impedances and the low signal levels to be detected, no conclusive results were obtained.

The first experiment attempted was to measure the successive peaks of the standing wave that exists on the line when it is driven by a sinusoidal generator. The set up for this experiment is shown in Figure 4-19. Due to the absence of enough fringe field, direct contact to the line had to be made. Finding the accurate location of the standing wave maxima was difficult due to the flatness of the maxima. The poor sliding contact on the line made it almost impossible to detect differences in the maxima with any consistency.

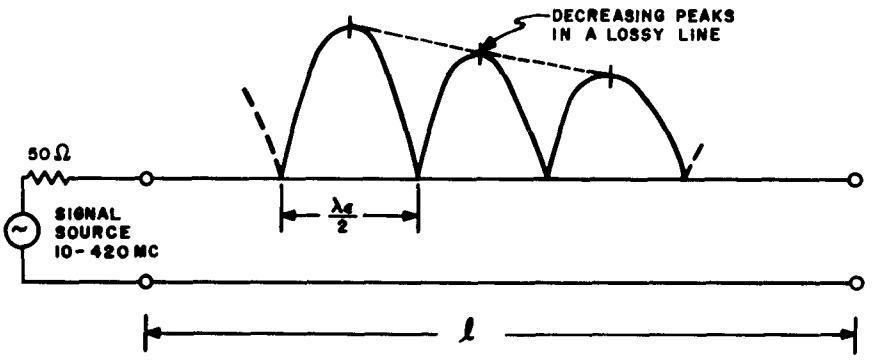


Figure 4-19. Attenuation Measurement

Another experiment which was tried was to observe the magnitude of the standing wave at the input point of a certain length of line at various frequencies. Utilizing this technique, the observed values should exhibit resonant peaks at regular frequencies intervals. If the line is lossy, the successive resonant peaks should decrease in amplitude and the attenuation constant can be calculated by the rate at which the peaks fall. The results of this experiment were also inconclusive because at about 80-100 mc, the transmission mode in the line showed an abrupt change. This condition rendered the usual transmission line formulas inapplicable. The plot of the readings taken by this test is shown in Figure 4-20.

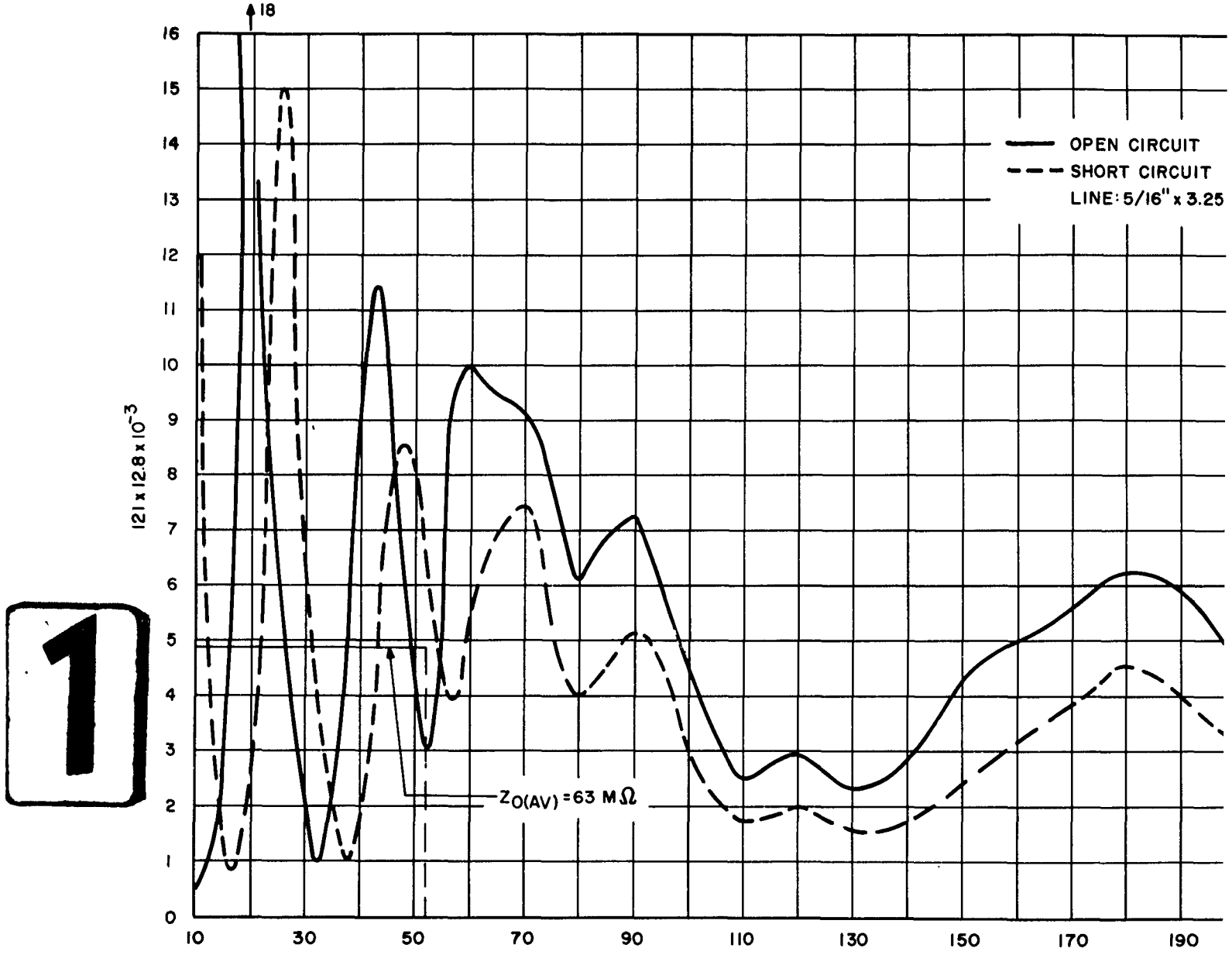
The third attempt to evaluate the frequency response of the line was to run a Fortran program on an IBM 709 computer. In this experiment, the line was pulsed with an SKL pulse generator and the input pulse waveform and the output pulse waveform were photographed. These waveforms were analyzed into their Fornier components by the program. By a comparison of the amplitudes at any given input frequency as well as the output, the response of the line can be derived. The program worked well, but again the results were not conclusive. The difficulty was the low repetition frequency of the SKL generator. Because of this limitation, extremely fine divisions in the time domain had to be measured accurately in order to extend the results to the higher frequencies of interest. When this was attempted the noise riding on the pulse became significant enough to produce spurious results, thus leaving the experiment inconclusive.

3. Experimental Tests of Low-Impedance Power Distrubition

By the use of Laplace transforms, it is possible to determine the amount of disturbance on a low-impedance power line when one monostable tunnel diode circuit fires. This disturb voltage was calculated to be of the order of 2-3 mv. An experimental set-up as shown in Figure 4-21 was designed to verify these results. It consists essentially of a string of six identical monostable circuits which are resistively coupled such that an input pulse will cause the first circuit to switch; the first circuit will in turn fire the second and so on down the string. The clamp tunnel rectifier associated with each circuit is connected to a 90-mv bias line. The bias line is essentially a 0.310-ohm characteristic impedance transmission line employing barium titanate as its dielectric. A 187B HP sampling oscilloscope was used to view the disburb voltage on this line when all six circuits were switching. Unfortunately, the noise level of this scope is approximately 2-3 mv itself and thus the disturb voltage due to the switching circuits was extremely difficult to detect. This experiment, however, did seem to verify the theoretically calculated values.

Figure 4-22a and b shows the close comparison between the noise level of the scope and the disturb voltage on the bias line. Figure 4-22a shows the actual noise level of the sampling scope while Figure 4-22b shows the disturb voltage on the line when all six circuits are switching.

Further experimentation will continue with this set-up whereby the circuits will be driven at higher frequency repetition rates in order to determine the magnitude of disturb voltage which can be expected on these bias line.


18
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
121 x 12.8 x 10^-3
10
30
50
70
90
110
130
150
170
190
OPEN CIRCUIT
SHORT CIRCUIT
LINE: 5/16" x 3.25
Z0(AV) = 63 MΩ

1

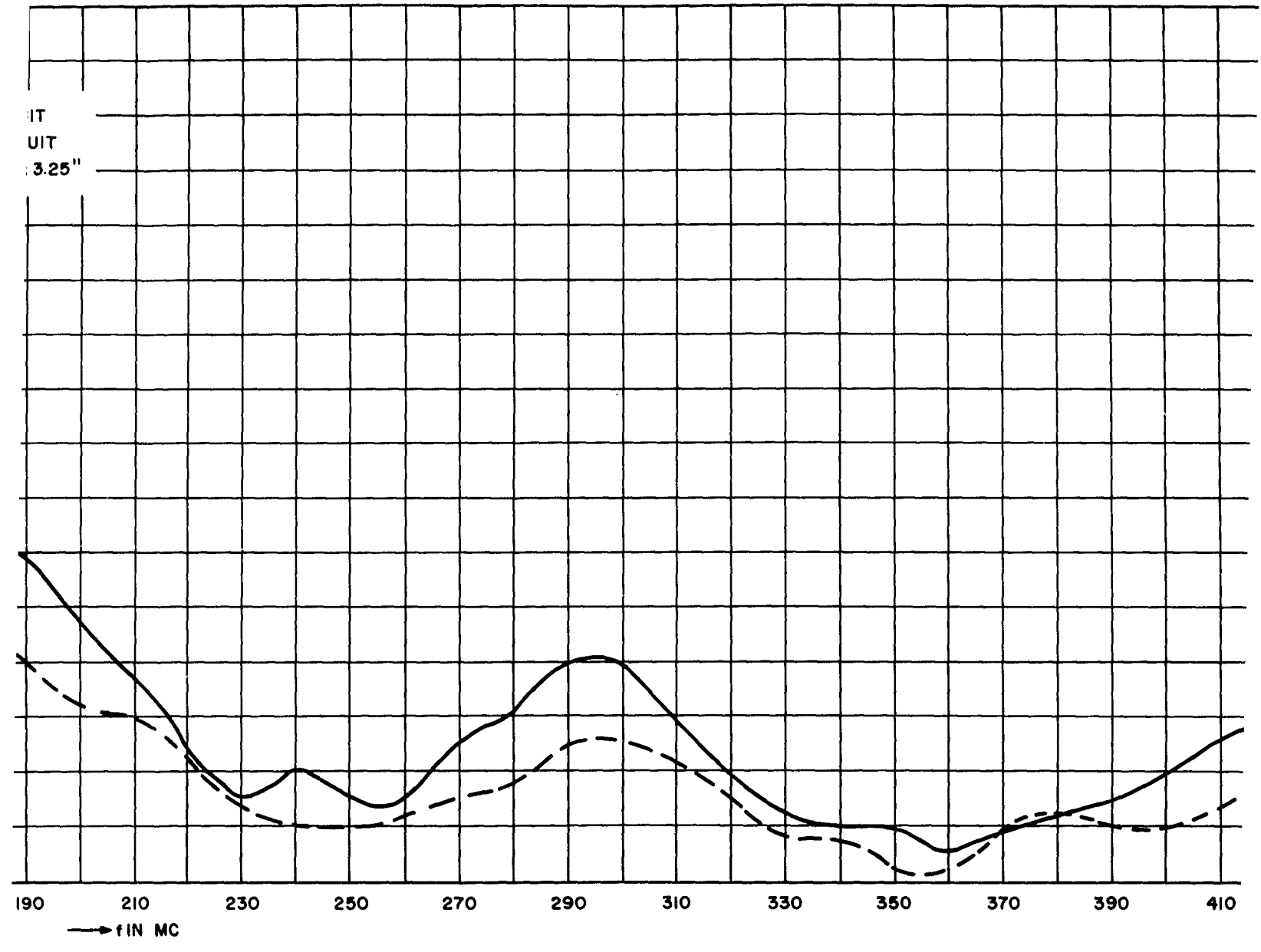


Figure 4-20. Results of Frequency Response Test

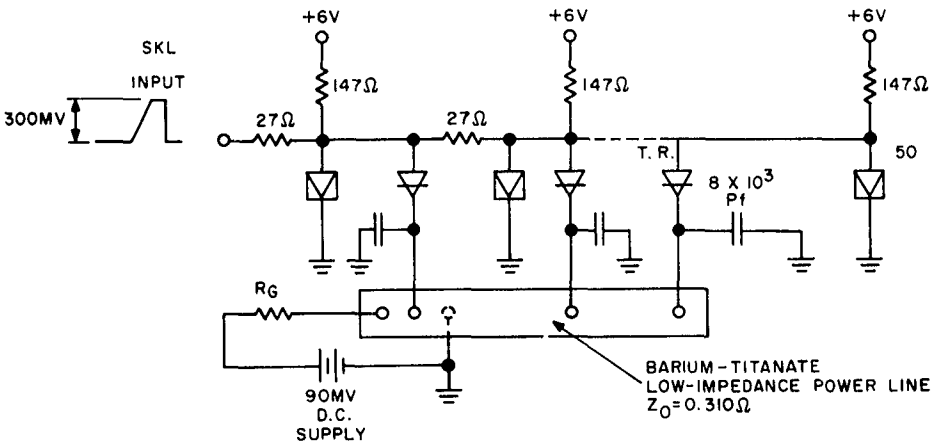


Figure 4-21. Noise Analysis Set-Up

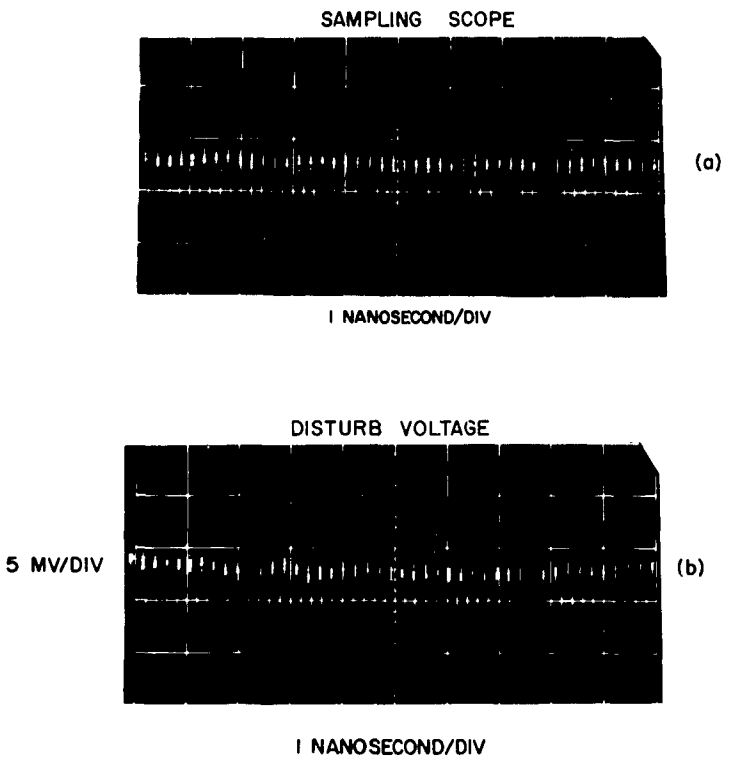


Figure 4-22. Comparison Between Noise Level of Scope and Disturb Voltage

F. POWER SUPPLY SPECIFICATIONS FOR TUNNEL DIODE SUBSYSTEM

A power supply is being designed to power only the logic circuits for the proposed tunnel diode subsystem. Although three different voltages are required, it is desired that all of these be contained on the same chassis. A-c power required to generate these voltages is to be fed directly from the mains.

The d-c output power requirements from the supplies are as follows:

Nominal Voltages (Volts)	Maximum Current (Amperes)	Total Regulation (%)
+6.0	26.0	±0.1
-6.0	6.0	±0.1
+.090	17.0	±1.0

Each supply will have a recovery or response time of 1 μs, i.e., each supply voltage can deviate from its regulated rating for a time not exceeding 1 μs for maximum transient load current variations. These maximum load current variations will be as follows:

+ 6-volt supply - 8 amps.

- 6-volt supply - 2 amps.

+90-mv supply - 3 amps.

All of the above current changes will be in the form of ramp functions having identical risetimes of 1 μs each.

The supply in general will also contain conventional equipment such as meters, jacks, overcurrent and overvoltage protection, etc.

G. SYSTEM DESIGN

System design continued this quarter with the following changes being instituted:

1. Console

   a) A start switch will initiate program operation.

   b) A stop switch will terminate the program at the end of the routine.

   c) A repeat switch will recycle the logic routine until the stop switch is set.

   d) An integrate switch will permit the combined operation of the memory and logic subsystems.

   e) A count allow switch which permits incrementing of the A register during each cycle of the logic routine.

   f) A parity error override switch will permit modification of the parity bit in the X register when a parity error is detected. When the parity bit is modified, the parity will be rechecked and if no error is detected, the logic routine will continue.

   g) A master clear switch will place each bistable circuit in its cleared position.

   h) A step switch will permit the system to step through a single logical sequence of commands and then place the system in a standby condition.

   i) A momentary contact resume switch will cause the logical routine to resume after the system has been placed in the standby condition as a result of the step switch being activated.

   j) A reset X switch will place the X register in its reset condition.

   k) For each stage of the X register, there will be a pushbutton to manually set the respective stages of the X register.

   l) A momentary contact switch will energize every indicator on the console for the purposes of checking lamp operation.

   m) The contents of each stage of the X and A register will be displayed. There will be two lights per stage indicating the condition of the output of each bistable half of the stage (lit when the stage is a "1").

   n) When in the step mode, an indicator will display the appropriate step in the sequence.

   o) All remaining bistable stages will have an associated indicator on the control panel which will be energized when their associated bistable stage is in the set position.

p) An error counter will indicate the number of parity errors obtained up to a limit of 16.

q) A clear switch will permit resetting the error counter to zero.

r) An output jack will be available for connection to a Berkeley Model 7350 EPUT meter to measure parity errors in excess of 16.

s) Coaxial jacks will be available to insert, from a pulse source, any of the commands of the logic subsystem.

A preliminary layout of the display and operating panel has been made, and the selection of switches and lights is under consideration. At present, the question of marriage circuit - display circuit compatibility is under investigation. It is expected that the console design for the test vehicle will be completed in about one month and the actual construction in about three months.

2. Logic

a. Circuits

Design of the logic subsystem is being based on the following circuits:

(1) Monostable AND gate

Input	1 Pulse	1 Level
Output	Two	

(2) Monostable OR gate

Input	Two
Output	Three

(3) Bistable

Set Input	Two
Reset Input	Two
Output	Three

(4) Active Delay Circuit

Input	One
Output	Two

(5) Load Wafer

Input	Eight

The load wafer is presently required to simulate tunnel diode loading for the 24-bit extension and the present bistable design requires that all bistables must be fully loaded.

b. Wafer Count

Each of the logic circuits will be placed on a single wafer 1.5-inches long. A savings of approximately 15% in the number of wafers required was realized when the change was made from the set-trigger type to the set-reset type of bistable circuit. The wafer count and their breakdown by logical functions is given in Table 4-2. The wafers required for fan-out of the control commands have been included in the wafer count of the register on which they act. This wafer count includes the wafers required for demonstrating the 24-bit extension capability, but does not include a four-stage error counter which if made from tunnel diode circuitry would require an additional eight bistable units, eight monostable AND units, four monostable OR units and one load wafer.

TABLE 4-2
WAFER COUNT AND FUNCTIONAL BREAKDOWN

Function	Control	X Register	A Register	Parity Checker	Subtotal
AND	30	22	31	17	100
OR	13	17	24	17	71
BISTABLE	12	12	10	6	40
DELAY	6	-	-	10	16
LOAD	3	1	2	2	8
	64	52	67	52	Total 235

3. Wafer Placement

As previously stated, each of the logic circuits will be placed on a single, 1.5-inch long wafer with the wafers placed 0.35 inch apart. To ease the problems of signal transmission, a restriction of six inches maximum length was placed on all transmission lines carrying pulses.

The change to the larger wafer and the six-inch restriction on all pulse leads necessitated an entirely new scheme of wafer placement from that outlined in IRR-10A and completed in the first part of this quarter. The new layout as shown in Figure 4-23 attempts to reduce the interconnecting wiring and still permit individual sub-frame testing of the principle functions of the logic subsystem.

The preliminary results of this layout indicate that the average transmission delay external to the wafer is approximately equal to 20% of the circuit delays. Using

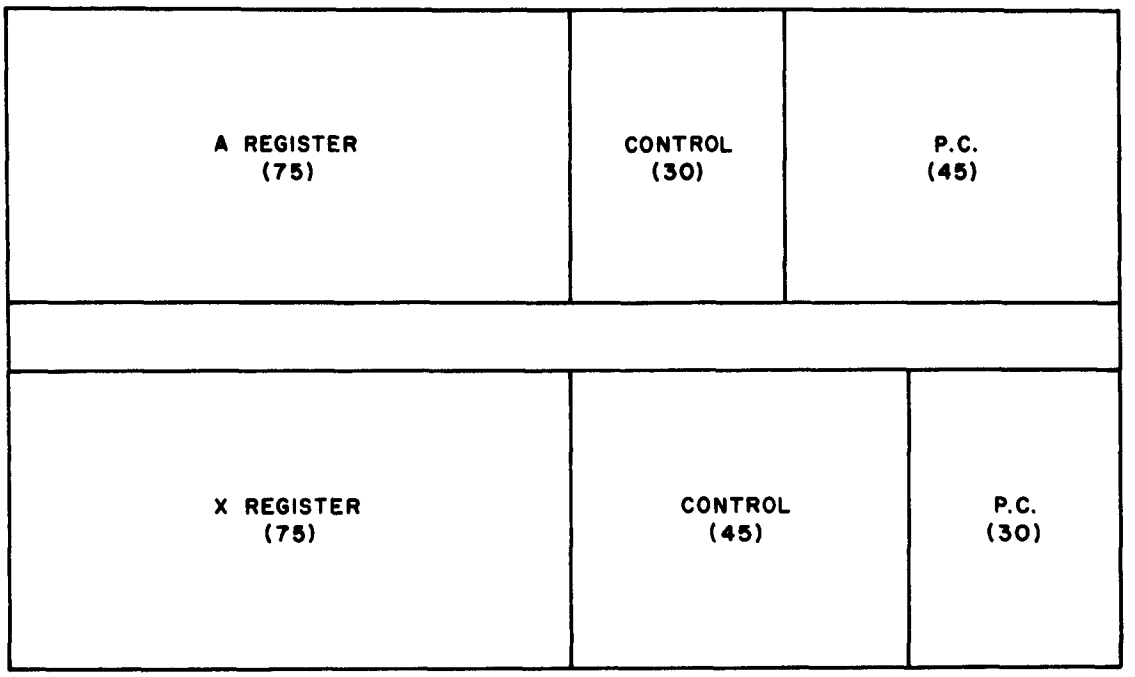


Figure 4-23. Preliminary Wafer Placement Scheme

this layout, there appears to be only two instances where the pulse transmission length exceeds six inches and line amplifiers (monostable OR's) must be inserted. The size of the logic subsystem is approximately 12 inches by 18.5 inches.

III. PROGRAM FOR NEXT INTERVAL

Investigation of faulty filter capacitors and of resistors changing value due to assembly will continue.

Design and development work on the low-impedance lines, as they will be used in the logic subsystem, has taken final shape by the end of this quarter. Further work on these lines will be mainly on methods of improving fabrication and on determining life performance.

Chapter 5. MEMORIES

SUMMARY

During the quarter, 18 of the 27 memory cells in the nine-word system have been operated at a repetition rate of 43 megacycles. The third plane will soon be activated, completing the system.

Fabrication of the 32-word system is approximately 30% complete, demonstrating fabrication techniques applicable to the 1024-word system.

Designs of peripheral circuits have progressed to the point where all components required from outside vendors have been ordered. Substitution of solution-grown diodes in peripheral circuitry to better utilize the memory cell's allowable operating area should not require any major circuit alterations.

Chapter 5. MEMORIES

I. PERSONNEL

The following personnel contributed to this phase of the project during the eleventh quarter:

G. Ammon
L. Dillon
M. M. Kaufman
P. Palamar
R. Reimertz
J. Schopp
L. Wu

II. DISCUSSION

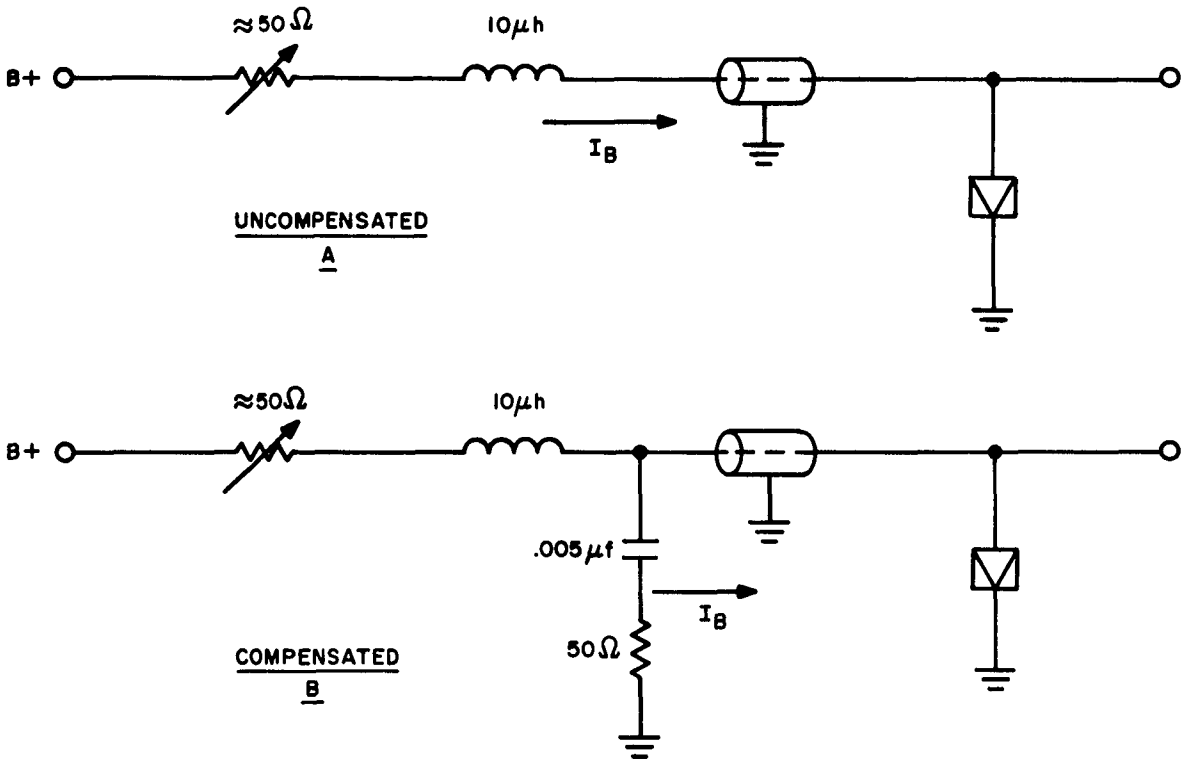
A. MEMORY SUBSYSTEM REVIEW

1. Nine-Word System

The nine-word, three-bit system is now being driven at 43 megacycles (23 nanosecond cycle time) with 18 cells activated and regenerating. There are two of the three proposed planes in the system, with the third plane soon to be installed.

The longest effort on the nine-word system was associated with operating the peripheral circuits together with the first plane and comparing calculated waveforms with laboratory results. The 43-megacycle repetition rate therefore was accomplished initially on only the first plane. This required modifying the original power distribution network so that it did not limit the repetition rate. The original power distribution network is shown in Figure 5-1. This method of supplying current was used to allow most of the dissipation to occur away from the circuits and to allow the magnitude of current bias to be changed conveniently. The large inductances associated with the power supply potentiometers made the bias current supplied to the circuit a sensitive function of the circuit repetition rate. At high repetition rates the circuit would not operate. By adding C_O and R_O the bias repetition rate sensitivity was significantly reduced.

The bias repetition rate sensitivity was studied by considering the current bias as a superposition of the current resulting from the B+ supply and by considering the current resulting from the tunnel diode switching as a pulse generator supply driving the bias network. It can be seen that the current contributed by the B+ supply alone is the same with both impedance networks; however, the tunnel diode switching produces a much less repetition rate sensitive current when driving the compensated network, as can be seen from the plot of Z vs. frequency. When the power distribution networks were impedance compensated, the first plane was driven at 43 megacycles. Circuit waveforms were carefully studied and compared to expected results. Operation of this circuit was considered satisfactory.



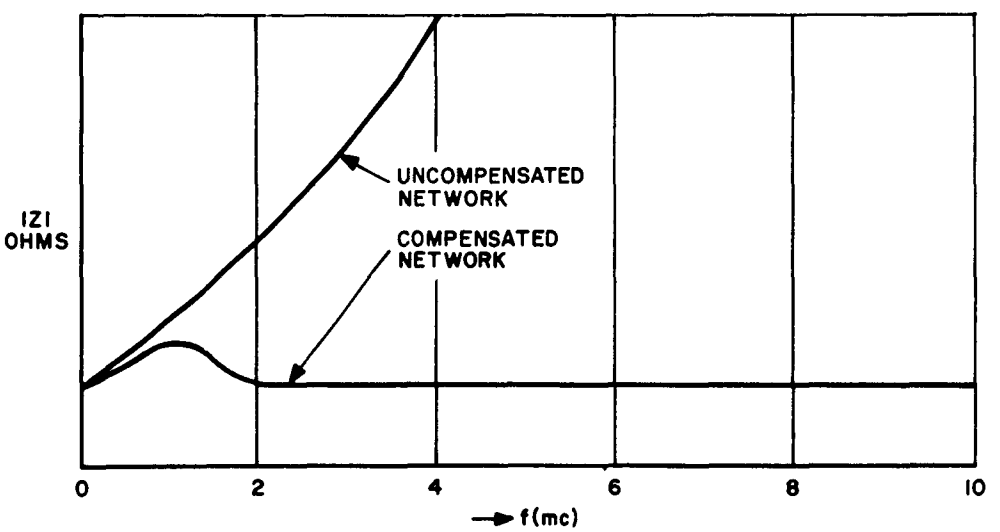


Figure 5-1. Power Supply Networks

The memory was set up for taking life data during periods when it was not in use. The memory has operated successfully for periods greater than 40 hours and has been run for a total of 300 hours without deterioration effects being observed. Placing the second plane in the system took only two weeks and it is anticipated that the third plane will be activated within an equal time period.

Waveforms from the nine-word memory are shown in Figure 5-2. Each pulse in the photograph represents the linear summation of three bits in a word, the bit information being represented by the digit driver outputs.

2. Fabrication

Fabrication of the 32-word system is approximately 30% complete. Figure 5-3 is a photograph of a plane for the 32-word system with the word and digit lines in place. The memory cell holder is shown in the corner of the photograph. The plane contains five digit lines and eight word lines for a total of 40 bits. The 32-word 5-bit system will hold four such planes. The space in the plane occupied by the memory cells does not exceed a 3 inch x 3 inch area; this is compatible with the simulation of a 32 x 32-bit plane with a .1 inch x .1 inch area per cell. In the 32-word system, the word driver diodes will be soldered directly into the word line and the additional area in the plane results from the word driver stages. The overall plane size then will be 3.5 inches x 4 inches.

The peripheral circuitry, in general, is being fabricated in a manner similar to that used for the nine-word system. The only difference is that the tunnel diode holders are now being made similar to the new memory cell holders.

It is of interest to compare the fabrication techniques being used in the extensibility portion of the memory program to the fabrication techniques used in the 32-word system. Figure 5-4 shows a mock-up model where the cell size is five times that of the actual proposed size. The transmission line structure is electrically identical to the 32-word system plane; however, the digit lines are placed beneath the plane so that all solder connections to the memory cell are accessible during construction. The memory cell holder is a molded piece having a volume of 0.1 inch x 0.1 inch x 0.2 inch. It contains two memory cells composed of two tunnel diodes, two tunnel rectifiers and two resistors. The fabrication techniques used in the extensibility program have shown themselves capable of production techniques and therefore constructed memory lines should be available within the second quarter of Phase IIIB.

3. Peripheral Circuits

Other than counting and decoding circuits, all memory circuits have been frozen to the point that components required from outside vendors have been ordered. The circuits have been frozen on the basis of driving fixed loads and being driven by fixed impedances. There are, however, approximations required in order to consider the circuits with fixed load and drive impedances, and it is now required that these approximations be eliminated. The extent of the, approximations becomes evident when it is realized that the circuits are either driven by or driving memory lines which have 32 cells attached.

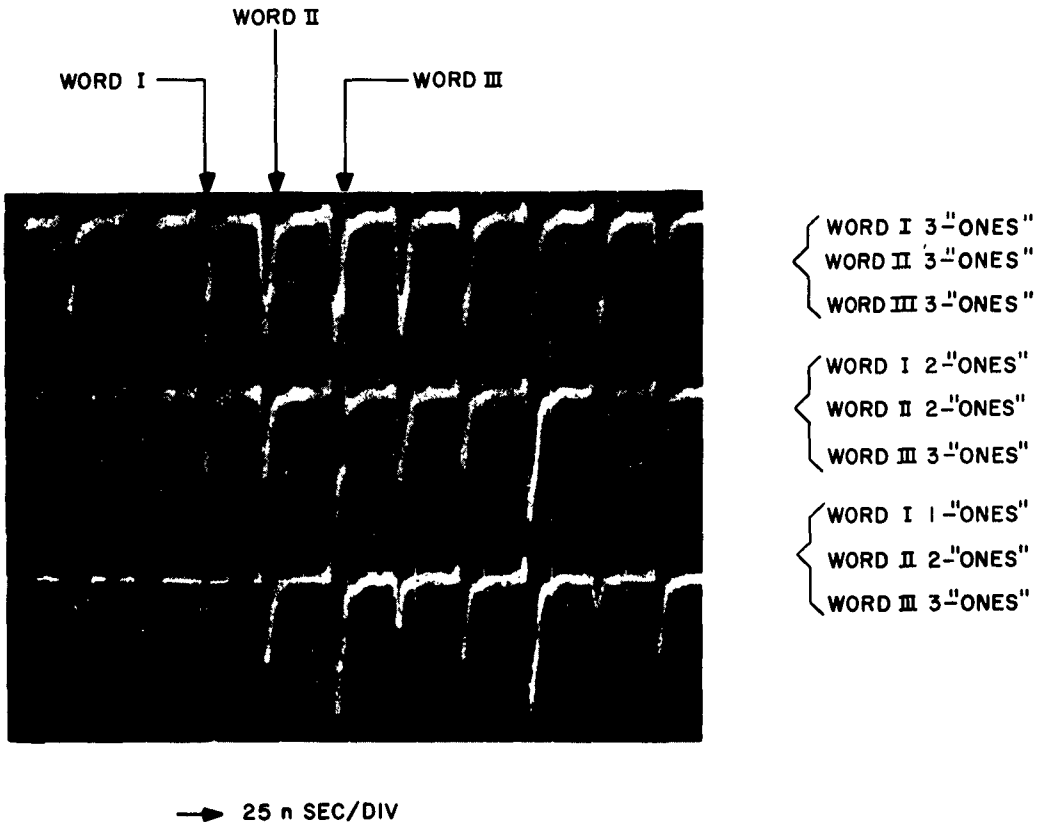


Figure 5-2. Memory Waveforms

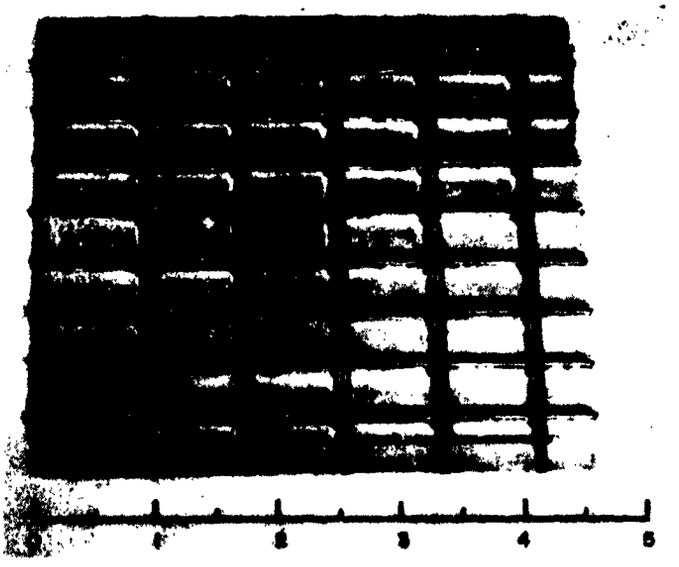


Figure 5-3. Memory Plane from 32-Word System

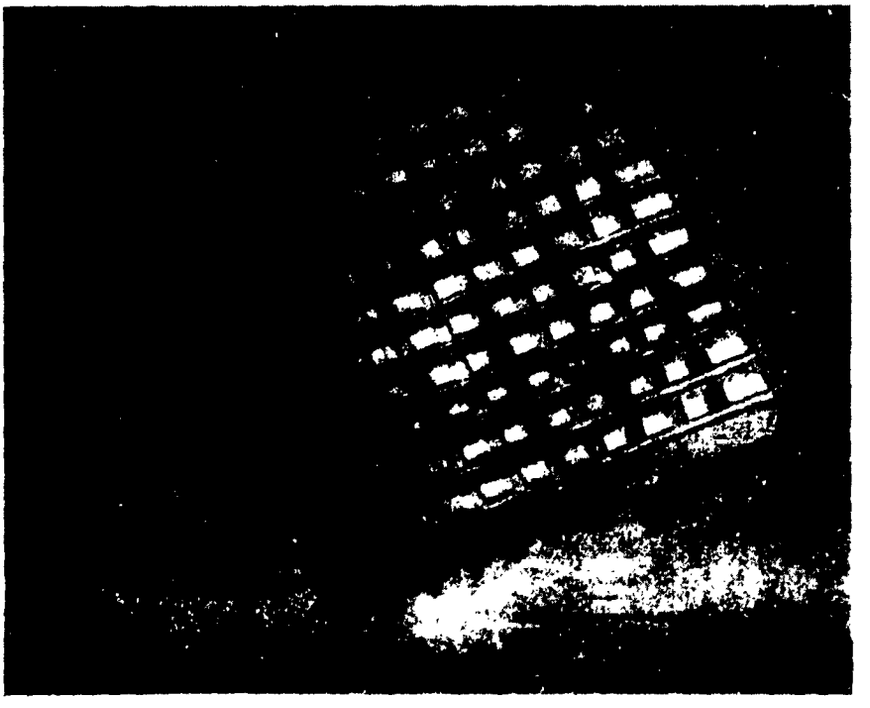


Figure 5-4. Model Showing Extensibility Fabrication Techniques

The lines, therefore, can have any of 2^{32} states. The circuits are now being refined as they are affected by specific information conditions. Furthermore, the load or drive impedances can be outputs from or inputs to other circuits which are completely unlike the circuits being designed and are in the process of being designed themselves. The final designs therefore, depend on the exact relationship between the final circuits. The circuits have been presently designed so that the only parameters which will be changed as the circuits are refined are the power supply voltages and inductance values which do not represent major overhauls.

The finalized circuits are shown in Figure 5-5. Another example of the importance of the relationship between circuits and refining designs occurs in the regeneration loop. If the recovery conditions of the circuits are such that the sense amplifier output resulting from the digit driver input can in turn fire the digit driver, the regeneration loop will oscillate. It is known, however, that in the nine-word system regeneration loop, oscillations do not occur, and the recovery time of the circuits are therefore in the proper ratio.

4. Memory Operation and GaAs Specifications

The most obvious and significant example of circuit relationships in the memory is between the memory cell and its drive-voltage requirements, together with the output voltage capabilities of the word and digit drivers.

Figure 5-6 illustrates the allowable operating region with respect to drive voltages. The triangular region defines all the word and digit line voltages which allow proper operation of the memory cell. However, the maximum word line drive voltage cannot be made as large as the maximum defined by this area because of the tunnel diode circuits. The usable area of operation is limited by the maximum word line drive voltage. The maximum word line voltage associated with circuits using GaAs diodes made by the diffusion process is 375 mv. The usable area then defined allows a maximum of 10% tolerance on the drive voltage shown. The maximum word line drive voltage associated with circuits using diodes made by the solution-grown process is 450 millivolts, allowing a 15% tolerance on the drive voltages. The revised nominal values are a word line voltage of 385 mv and a digit line voltage of 530 mv.

The GaAs units originally supplied were made by the diffusion process and circuits were designed using these diodes. The specifications on the GaAs diodes made by the diffusion process were frozen in July. However, an improvement in the manufacture of diodes made by the solution-grown process has allowed their use in the drive circuits. The new circuit designs for accommodating solution-grown diodes require only a slight change in the d-c bias voltages. The new circuits have been finalized to the point where all components required from vendors have been ordered.

B. MEMORY CELL TOLERANCE ANALYSIS

1. General

The d-c characteristics of the tunnel diode and tunnel rectifier have been used to determine an allowable operating region with respect to drive voltages on the digit and word lines. It remains for this work to be substantiated through dynamic analysis with practical voltage waveforms being considered.

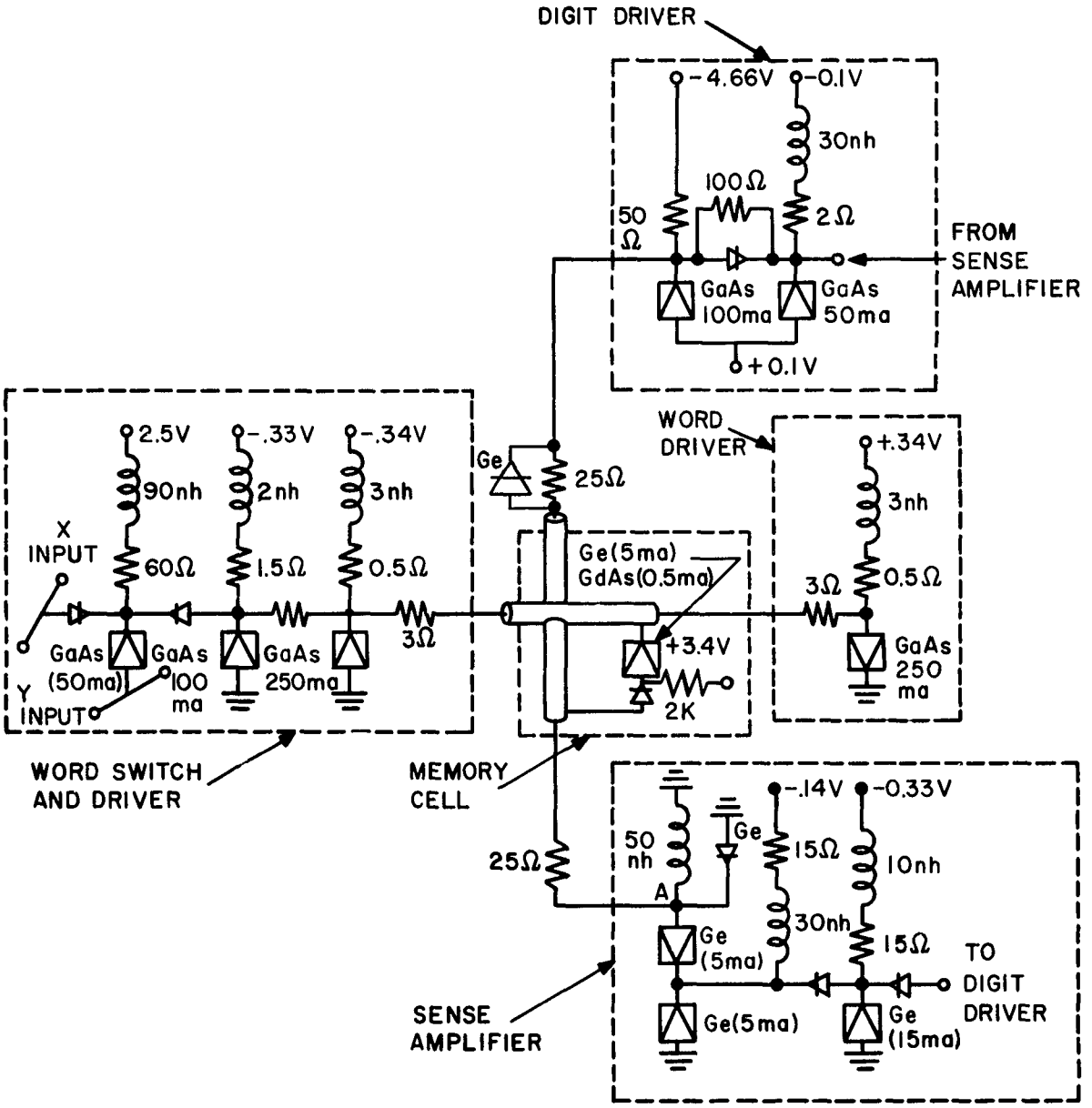


Figure 5-5. Finalized Memory Circuits

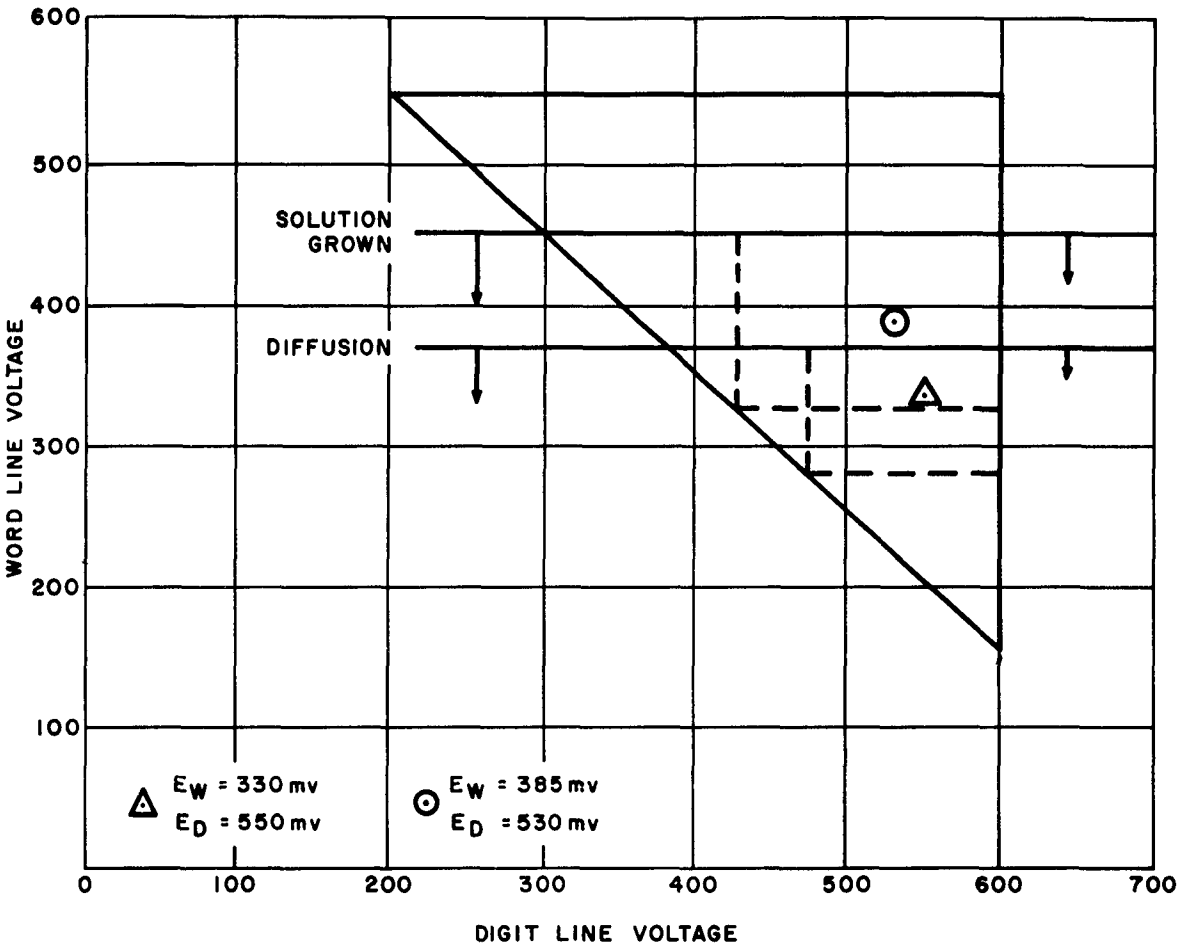


Figure 5-6. Memory Cell Operating Region

2. Read Operation

The read operation may be treated separately since it does not enter into determining the memory cell's allowable area of operation. It is only necessary to specify a read-word driver output which is sufficient to switch the tunnel diode from the low to high voltage state. Figure 5-7 illustrates the switching path on the tunnel diode's I-V characteristic under worst-case operating conditions. The numbers along the trajectory indicate the time which has passed as each point along the path is reached. Two positions of the tunnel rectifier I-V characteristic relative to the tunnel diode are shown. The analysis was carried out to the point where a steady state switching path toward the new quiescent operating point was established. All parameters listed represent a worst-case condition for the read operation with the exception of the stray series inductance, L, which will require further study in order to determine limits.

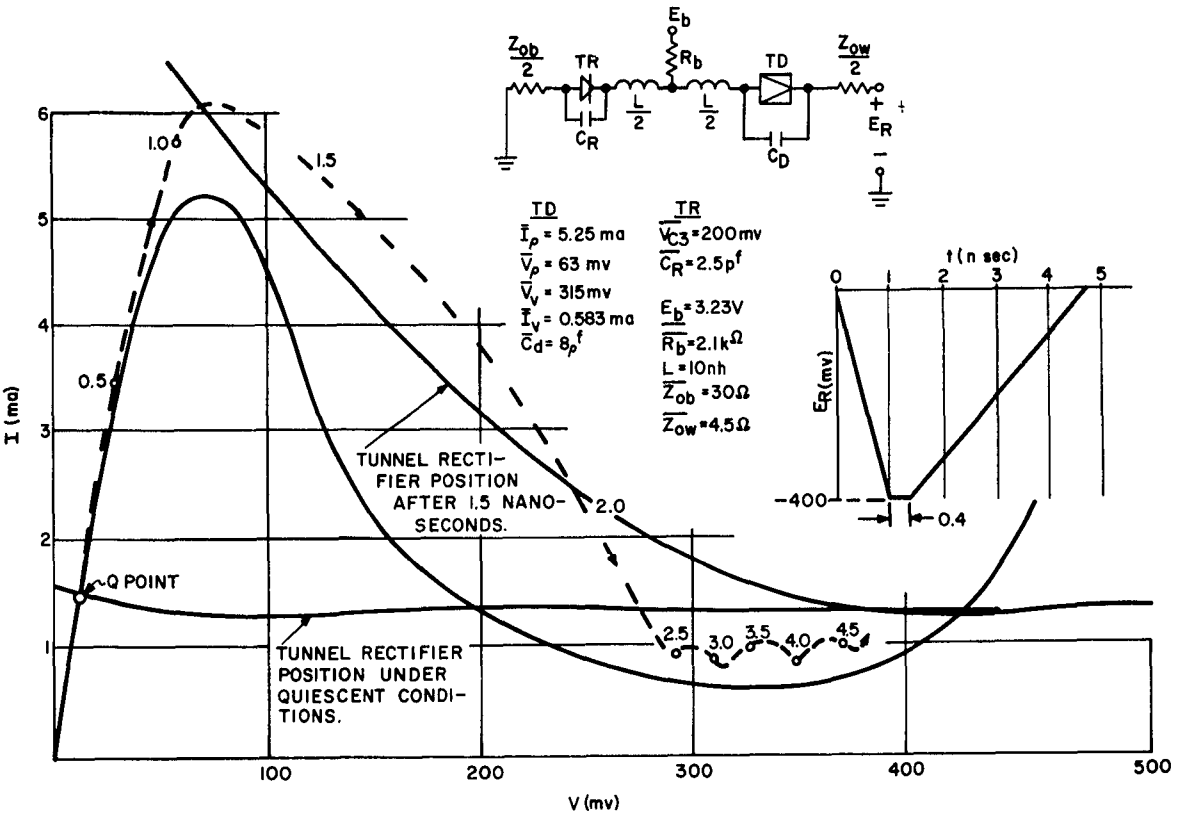


Figure 5-7. Read Operation

3. Half-Select

A half-select word line trajectory is shown if Figure 5-8. The tunnel rectifier characteristic is shown relative to the tunnel diode under quiescent conditions and after 1.4 nanoseconds when the applied voltage E_W is at its maximum. It can be seen that the current contributed by capacitive feedthrough is very significant since the rectifier is operating in the high-impedance region. The operating path indicates some ringing is present when the non-linear elements are operating in their high differential-resistance region. The ringing is due to the series RLC circuit formed by L, C_r, and C_d, and the transmission line terminating resistors.

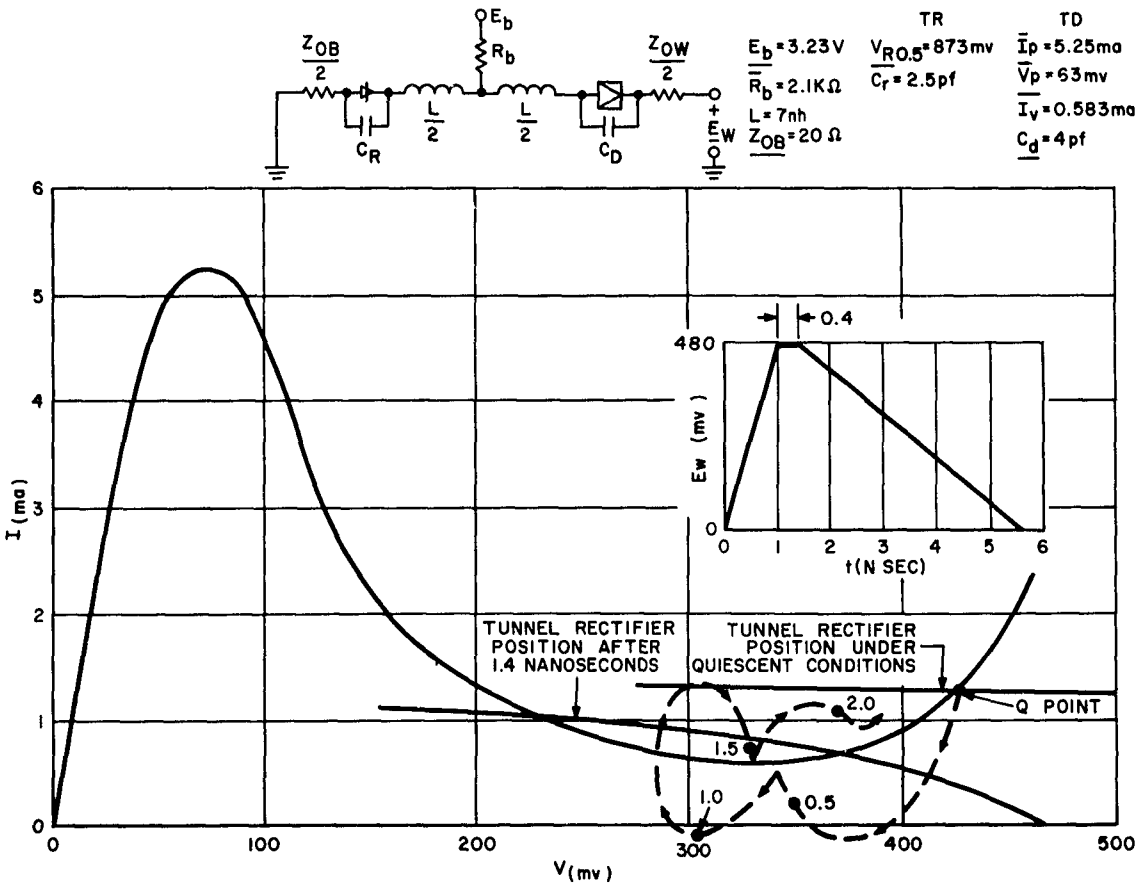


Figure 5-8. Half-Select Word Line

Figure 5-9 illustrates the trajectory under worst-case conditions of half-select, digit-line operation. When the two half-select operations are compared, it is apparent that the digit line case is most severe because the voltage magnitude is greater, the output is longer in duration, and $^{dv}/_{dt}$ is greater, increasing the chance of discharging the tunnel diode capacity. The cell did not switch to the low voltage state, substantiating the limit condition shown in the figure labeled "Memory Cell Operating Region." Since the cell did not switch under digit line conditions, there is no change of switching occurring on the word line. It is possible that the allowable operating region might be extended even beyond the 600-mv limit determined from the static analysis. Future work in half-select will be directed toward determining how much farther the limit may be extended.

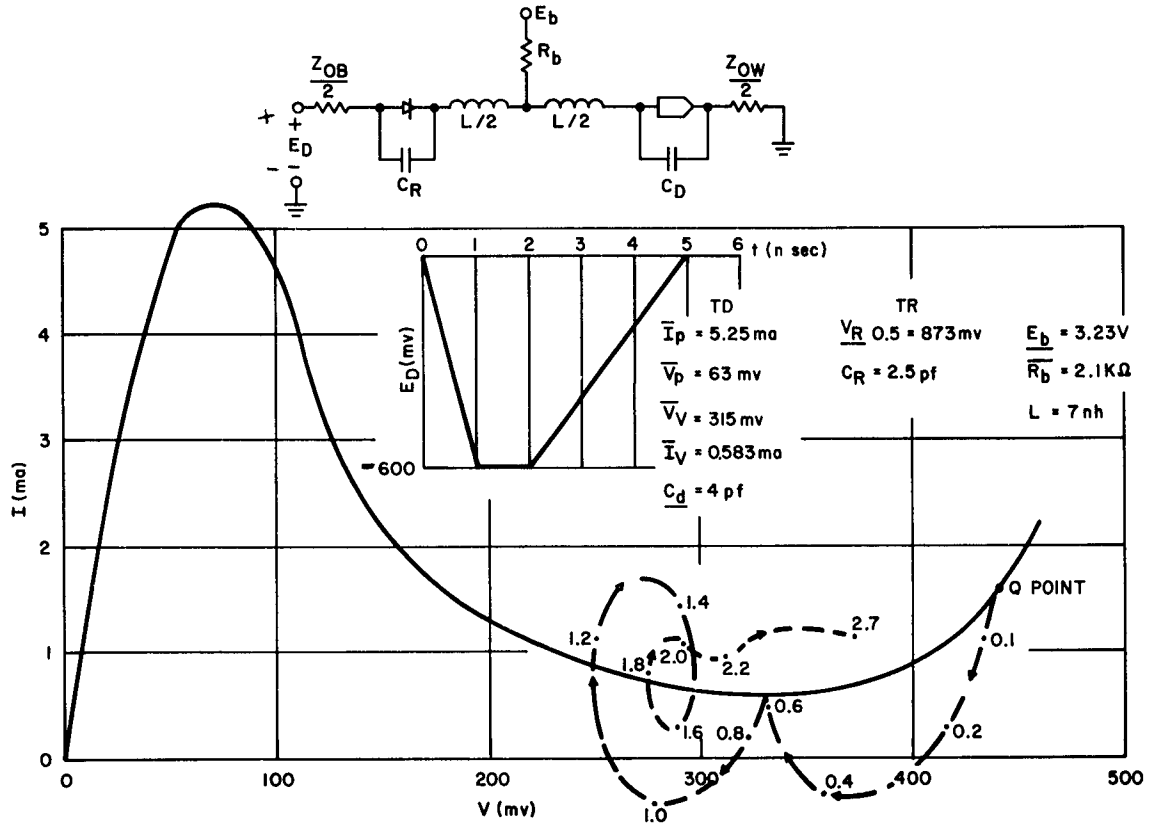


Figure 5-9. Half-Select Digit Line

4. Write Operation

A dynamic analysis of the write operation is shown in Figure 5-10. The trajectory shows that switching to the low voltage state was not accomplished. This was expected since the sum of the digit and write voltage was not sufficient to cause operation in the allowable operating region. Work in progress indicates that the operating region may be modified since it appears that larger voltages may be required to switch the cell than was originally indicated by the static analysis.

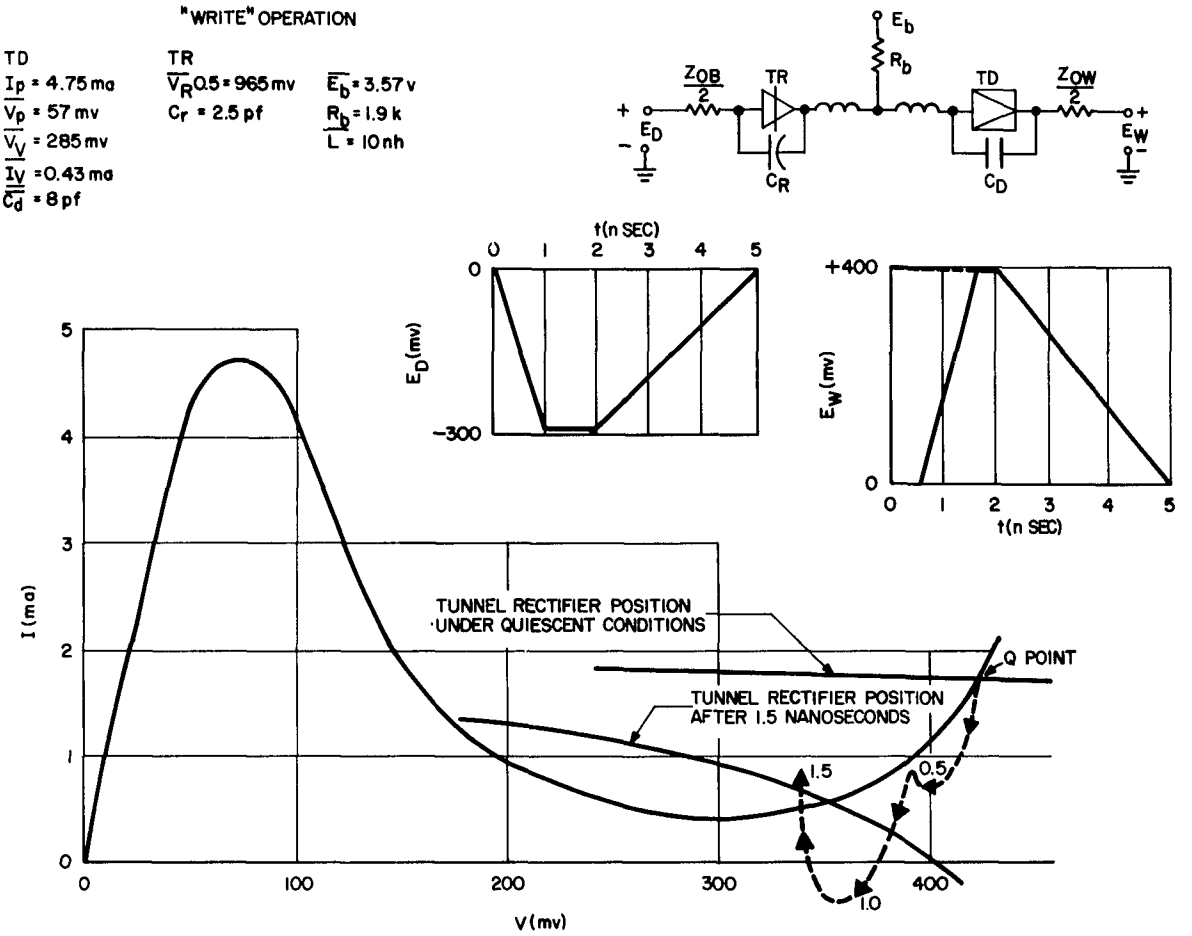


Figure 5-10. Write Operation

C. WORD SWITCH AND DRIVER STUDY

1. General

A dynamic analysis of the a two-stage word switch and driver and a d-c analysis of a three-stage version of this circuit were completed during this quarter. The conditions and results of both analysis are stated here plus an outline of the procedure used in the dynamic analysis. The procedure used for the d-c analysis is similar to that described in IRR-10A except graphic means rather than equations were used in some cases, such as the case where the half-select switching currents were desired.

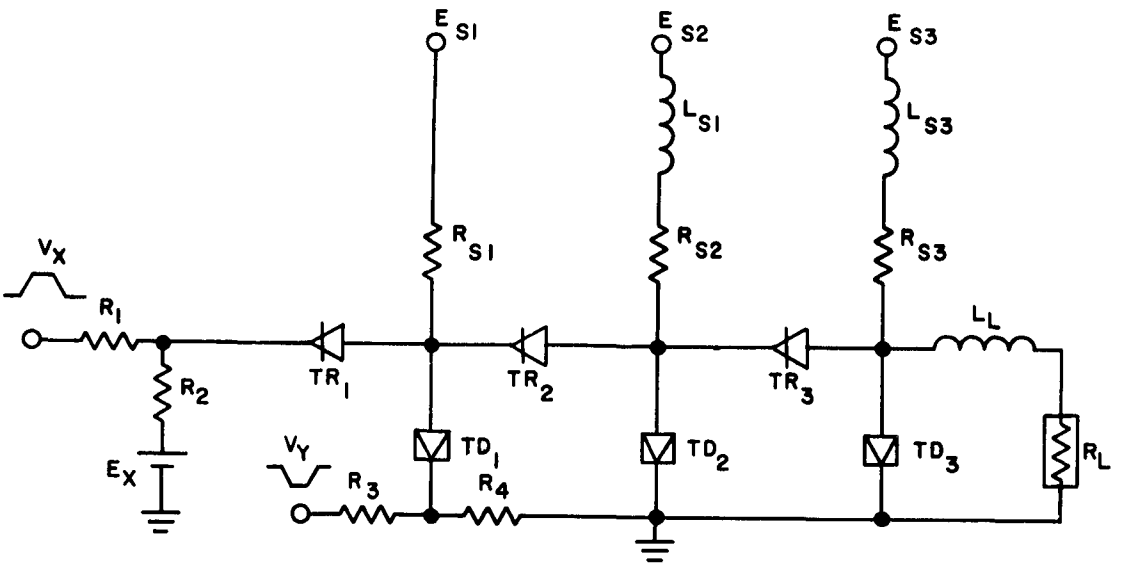


Figure 5-11. Three-Stage Word Driver Circuit

2. D-C Analysis

A d-c analysis was made of the three-stage word switch and driver circuit. Figure 5-11 shows the circuit with all the parameters whose values were determined by this analysis. The nominal values of these parameters and the tolerances assumed are given in Table 5-1. Although these are in general the widest possible tolerance that the d-c analysis and the results of the two-stage analysis will permit, when all the inductances are optimized the dynamic analysis of this circuit may permit increasing the tolerances of the second and third stage. The tolerances of the first stage are dictated almost entirely by the d-c analysis since there is no inductance in this stage and the trajectory cannot go beyond the load line. If inductance is included in this stage and provided the duty cycle is low, it may be possible to increase these tolerances. In this analysis the half-select currents on the switching line for each word driver was limited to 1.5 ma for the worst case.

TABLE 5-1

PARAMETERS AND TOLERANCES FOR D-C ANALYSIS OF THREE-STAGE WORD SWITCH AND DRIVER CIRCUIT

RESISTOR	VALUE (OHMS)	TOLERANCE
R_1	8	2% for DC. 5% for A.C.
R_2	8	2% for D.C. 5% for A.C.
R_3	3	± 2%
R_4	3	± 2%
R_{s1}	110	± 2%
R_{s2}	1.5	± 2%
R_{s3}	.5	± 2%
R_1	6	± 10%

SUPPLY VOLTAGE	MILLIVOLTS	TOLERANCE (%)
E_x	305	± 3
E_{s1}	4880	± 2
E_{s2}	325	± 3
E_{s3}	340	± 3

SWITCHING VOLTAGE	MILLIVOLTS	TOLERANCE (ON THE LINE) (%)
V_x	750	± 10
V_y	750	± 10

TUNNEL DIODES	I_p (MA)	V_p (MV)	V_v (MV)	I_v (MA)	V_f (MV)
1	50 ± 2%	160 ± 5%	540 ± 7%	5 max	1100 ± 7%
2	100 ± 3%	210 ± 5%	575 ± 7%	10 max	1120 ± 7%
3	250 ± 3%	240 ± 5%	575 ± 7%	25 max	1135 ± 7%

TUNNEL RECTIFIERS	I_p (MA MAX)	V_f (MV)	V_r at 10 MA (MV)	V_c at 10 MA (MV)
1	1	410 ± 5%	483 ± 5%	68 ± 5%
2	1	410 Min	483 Min	68 ± 5%
3	1	389.5 Min	459 Min	68 ± 5%

3. Dynamic Analysis

A dynamic analysis was made on a two-stage, tunnel diode word driver. This analysis was based on the worst case for switching. Thus, the results described in the following text indicate the minimum output available for the load used in this analysis. More output current could be obtained if the inductor in the load branch was decreased. A partial analysis was made for a 5-nh inductor in the circuit and it was found that the second-stage trajectory would clear the peak of the second stage tunnel diode. The analysis was not carried much beyond the peak of the tunnel diode; but it is felt that with this circuit change, this stage could switch yielding more output current and could reset slightly faster.

Since the analysis made was worst case for switching, it was not the worst case for resetting. This means that the circuit may take more time to reset in some other case. However, a worst case for resetting would be a good case for switching. Thus, switching time would be reduced and the overall cycle time might not change very much.

In this analysis the tunnel rectifier capacitances and inductances as well as the tunnel diode inductances were not considered because of the added complexity these elements would present to the analysis. Also, the risetime of the switching voltages was neglected, but it is felt that this would only increase the cycle time by whatever risetimes could be realized.

No tolerances were put on the tunnel diode capacitances or the circuit inductors. The analysis showed that the value of the diode capacitances is not too critical, thus the values used could be taken as nominal and a reasonable tolerance assigned to them. The inductors used were almost optimum for switching. It is felt that it would be good to reduce the load inductor to 5 nh; however, this is almost a minimum value. The second stage source inductor, L_{s2}, is even more critical. When this inductor was reduced to 2.5 nh, the second stage would not switch. Therefore, any tolerance assigned to this inductor should keep the minimum possible value to that used in this analysis.

The procedure for this dynamic analysis was as follows (refer to Figure 5-12):

(a) All quiescent operating states of the diodes and rectifiers were obtained from the d-c analysis.

(b) A voltage and current V_d and I_d, was assumed.

(c) $V_1 = I_d R'_{34} + V'_{34} + V_d - V'_y$ was determined.

(d) $I_{s1} + I_1$ was determined from V-1 characteristic constructed for these two branches.

(e) $I_t = I_{s1} + I_1 - I_d$ was determined.

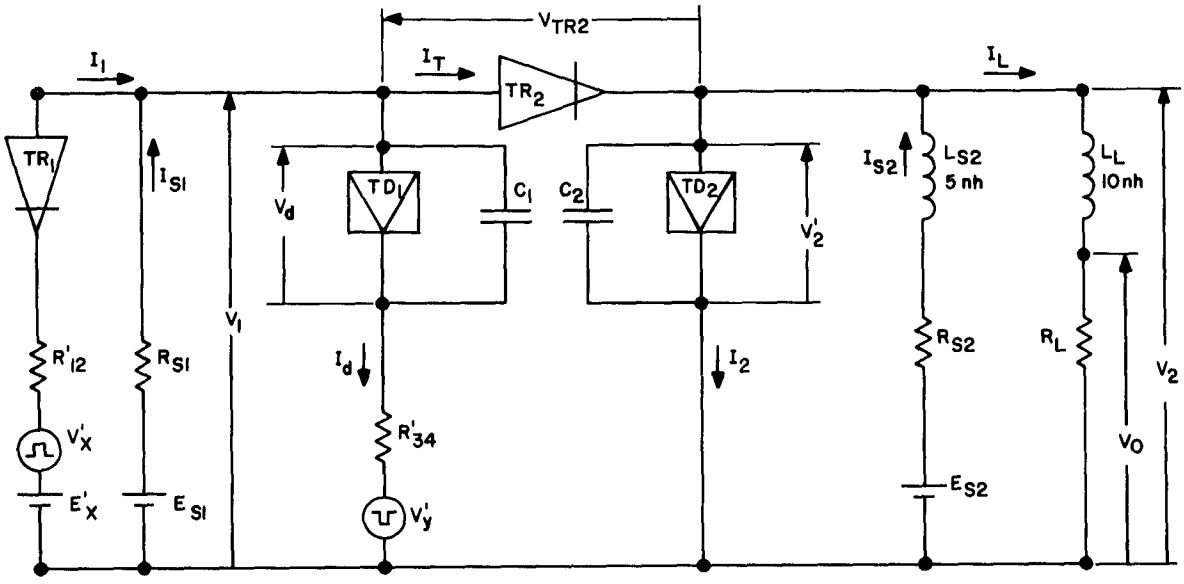


Figure 5-12. Equivalent Circuit of Two-Stage Driver

(f) V_{tr2} was determined from tunnel rectifier characteristic at I_t.

(g) $V_2 = V_1 - V_{tr2}$ was determined.

(h) I_{s2} was determined from graph of I_{s2} vs. V_2

(i) I_1 was determined from curve of I_1 vs V_2. (Here graphical construction must be used because of inductor L_{s2}).

(j) I_L was determined from the curve of I_1 vs V_2.

(k) $I_2 = I_t + I_{s2} - I_1$ was determined.

(l) V_2' was determined from curve of V_2' vs. I_2. (Graphical construction must be used because of capacitor C_2 across TD_2).

If $V_2' = V_2$, the assumption originally made was correct since all circuit equations have been satisfied.

a. Dynamic Analysis Specifications

The specifications used in the dynamic analysis are given in Table 5-2 below:

TABLE 5-2
SPECIFICATIONS FOR DYNAMIC ANALYSIS OF TWO-STAGE WORD DRIVER CIRCUIT

Item		Nominal	Tolerance	Worst Case for Switching	Unit
R'_{12}	equiv. imped. - line & termination	6.25	±2%	6.25	ohms
R'_{34}	equiv. imped. - line & termination	1.5	±2%	1.5	ohms
R_L	equiv. imped. line & termination	6	±10%	5.4	ohms
R_{s1}		138	±2%	140.76	ohms
R_{s2}		.50	±2%	.51	ohm
V'_x	equiv. switching voltage	420	±12%	370	mv
V'_y	equiv. switching voltage	-375	±12%	-331	mv
E'_x	equiv. biasing voltage	171	±4%	171	mv
E_{s1}		6000	±2%	5880	mv
E_{s2}		320	±2%	313.6	mv
C_1		25	None Specified	25	pf
C_2		115	None Specified	115	pf
L_1		10	None Specified	10	nh

TABLE 5-2
SPECIFICATIONS FOR DYNAMIC ANALYSIS OF TWO-STAGE WORD DRIVER CIRCUIT (Continued)

Item	Nominal	Tolerance	Worst Case for Switching	Unit
L_{s2}	5	None Specified	5	nh
Tunnel Diode #1				
I_p	50	±2%	51	ma
V_p	160	±5%	168	mv
I_v	3.9	±5%	4.1	ma
V_v	500	±5%	525	mv
V_f	1127	±5%	1070	mv
Tunnel Diode #2				
I_p	250	±2%	255	ma
V_p	202	±5%	212	mv
I_v	15.6	±5%	16.4	ma
V_v	553	±5%	572	mv
V_f	1150	±5%	1092	mv
Tunnel Recitifier #1				
I_p	1	max.	1	ma
V @ 10 ma	70	±5%	73.5	mv
V @ -10 ma	485	±5%	510	mv
V_f	410	±5%	432	mv
Tunnel Rectifier #2				
I_p	1	max.	1	ma
V @ 10 ma	70	±5%	73.5	mv
V @ -10 ma	510	±5%	484	mv
V_f	432	±5%	410	mv

b. Results of Dynamic Analysis'

The results of the dynamic analysis are illustrated in Figure 5-13 where the output voltage is shown as a function of time. The input switching voltages are also shown with time being measured from the instant these voltages are applied.

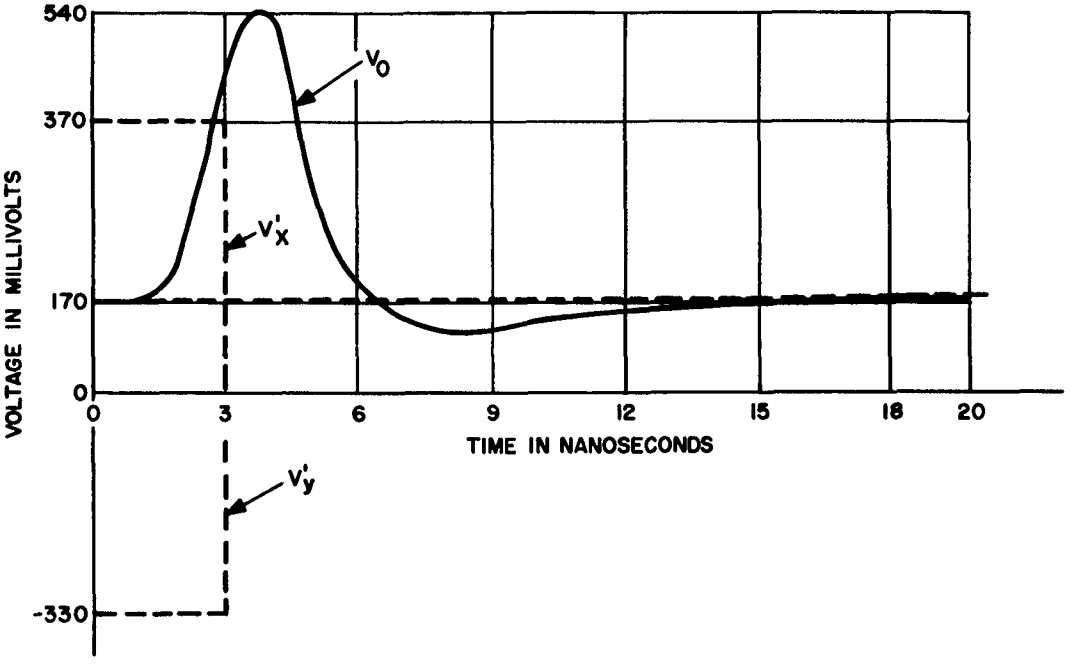


Figure 5-13. Output and Switching Voltages vs. Time for Two-Stage Driver

As can be seen the output pulse is short in duration compared to the time it takes the load voltage to return to its quiescent value. This long recovery time is due to the inductors in the second stage. By reducing these, the recovery time can be reduced. However, there is a limit to the amount of reduction that can be used because some inductance is necessary to allow the second stage to switch. Thus there is some optimum inductance that will produce the shortest recovery time with a certain minimum required output.

D. DIGIT DRIVER TOLERANCE ANALYSIS

1. General

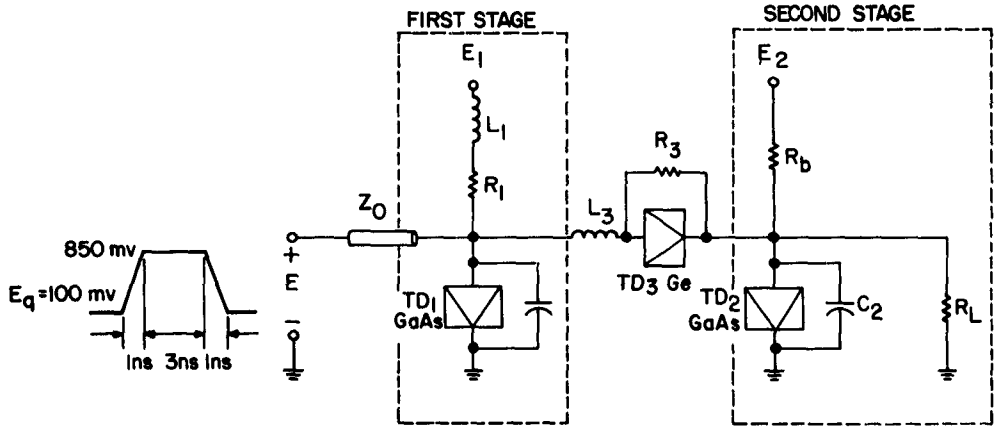
The dynamic analysis of two worst cases (switching and resetting of TD_2) was completed. The nominal case was also studied in view of contrasting the two extreme situations. The combination of tolerances on each component which brings the quiescent point farthest from the diode peak current constitutes the worst-case switching. On the other hand, the opposite-extreme tolerances of these components

co-establish the worst-case resetting, and the diode is biased closest to its peak.

V-T curves under each case were compared, and as a result, the digit driver output was seen to meet the requirements satisfactorily.

It is to be noted that in this graphical analysis, the adjustments necessitated for the incremental changes in voltage and current relating the two stages (discussed in IRR-10A) is applied.

The digit driver circuit with the nominal values and tolerances of each component is shown in Figure 5-14.



$E_1 = 218$ mv ± 3%
$L_1 = 25$ nh
$R_1 = 2\Omega \pm 2\%$
$Z_0 = 50\Omega \pm 10\%$
$C_1 = 25$ pf

$L_3 = 3$ nh
$R_3 = 100\Omega \pm 2\%$

$E_2 = 5500$ mv ± 2%
$R_b = 50\Omega \pm 2\%$
$R_L = 8\Omega \pm 10\%$
$C_2 = 50$ pf

TD1
$V_{p1} = 160$ mv ± 5%
$I_{p1} = 50$ ma ± 3%

TD3
$V_{p3} \cong 50$ mv
$I_{p3} = 1$ ma
V_C at 60 ma = 205 mv ± 7%
$V_f = 410 \pm 5\%$
V_R at 10 ma = 483 ± 5%

TD2
$V_{p2} = 160$ mv ± 5%
$I_{p2} = 100$ ma ± 3%

Figure 5-14. Digit Driver Circuit

2. Dynamic Analysis

a. Nominal Case

Zero risetime of the input signal to the driver is considered in this case so that its negligibility and its effect on the dynamic characteristic of the circuit can be studied. The risetime at the output is then seen to be 0.4 ns faster than that of considering 1-ns rise at the input.

Henceforth, a definite rise and fall time of 1 ns each, which is the waveform seen at the output of the sense amplifier, was decided to be applied for the whole-analysis. A sliding load line was therefore used in the first stage.

Switching trajectories of the first and second stages are shown in Figures 5-15 and 5-16, respectively. The output waveforms for these stages are shown in Figure 5-17.

b. Worst Case Switching

This situation occurs with the combination of the following parameters:

First Stage: E_q, $\overline{Z}_o$, $\underline{E}_1$, $\overline{R}_1$, L_1, C_1, $\overline{V}_{p1}$, and $\overline{I}_{p1}$
Second Stage: $\underline{E}_2$, $\overline{R}_b$, $\underline{R}_L$, C_2, $\overline{V}_{p2}$, and $\overline{I}_{p2}$

$\overline{R}_3$ is combined with TD_3 which is considered as the non-linear load line of the second stage. A stray inductance of 3 nanohenries in series with TD_3 is included.

Figures 5-18 and 5-19, respectively, show the switching trajectories of the first and second stages for this situation. The associated outputs for both stages are shown in Figure 5-20.

c. Worst Case Resetting

Opposite to the extremes listed in 2.b. above, this situation occurs with the combination of:

First stage: E_q, $\underline{Z}_o$, $\overline{E}_1$, $\underline{R}_1$, L_1, C_1, $\underline{V}_{p1}$, and $\underline{I}_{p1}$
Second stage: $\overline{E}_2$, $\underline{R}_b$, $\overline{R}_L$, C_2, $\underline{V}_{p2}$, and $\underline{I}_{p2}$
TD_3: $\underline{R}_3$

The switching trajectories of both stages are shown in Figures 5-21 and 5-22, respectively. The associated outputs for both stages are shown in Figure 5-23.

3. Summary

The digit driver outputs under different cases are categorized and tabulated in Table 5-3 (refer to Figure 5-24).

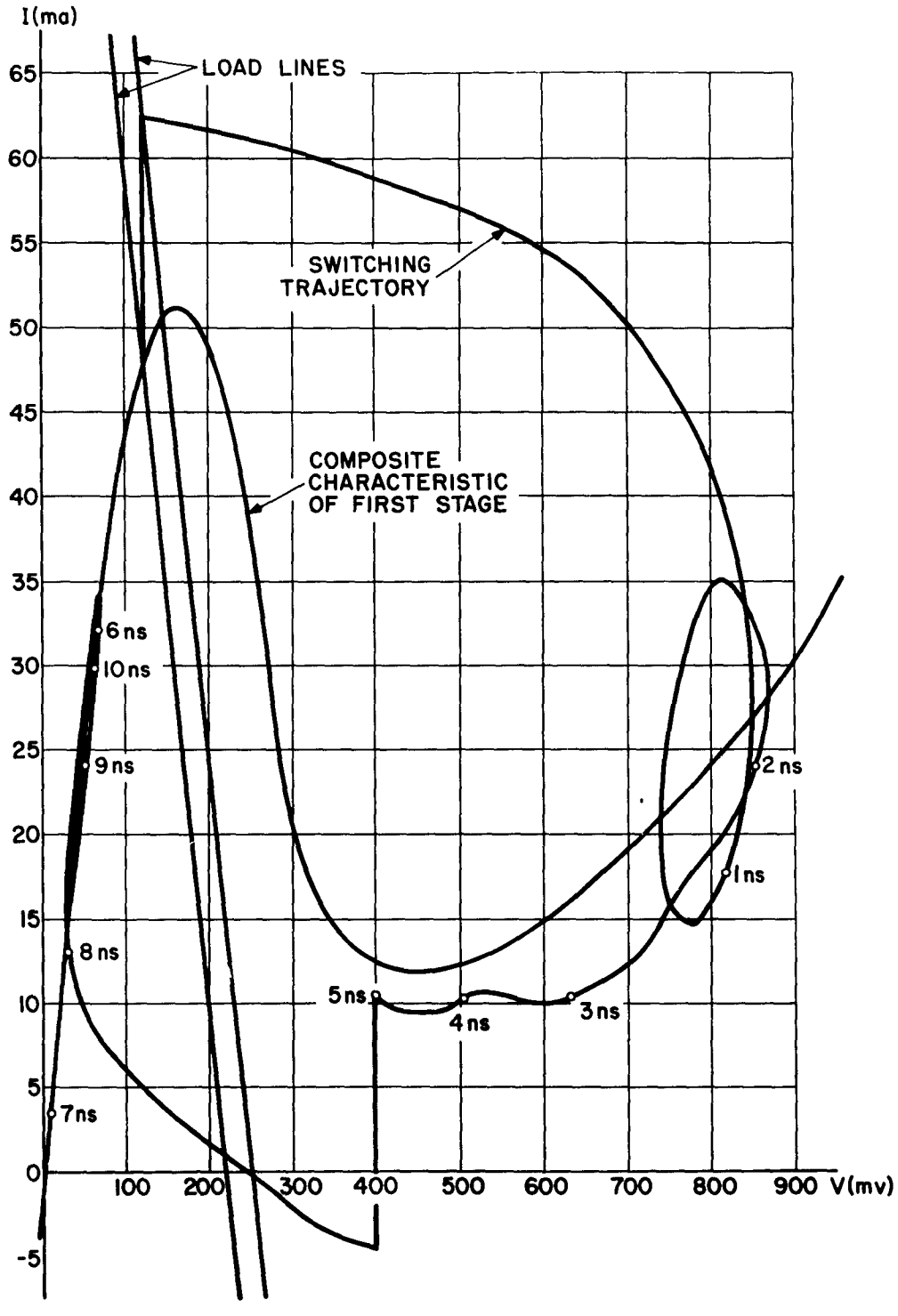


Figure 5-15. Switching Trajectory of First Stage, Nominal Case

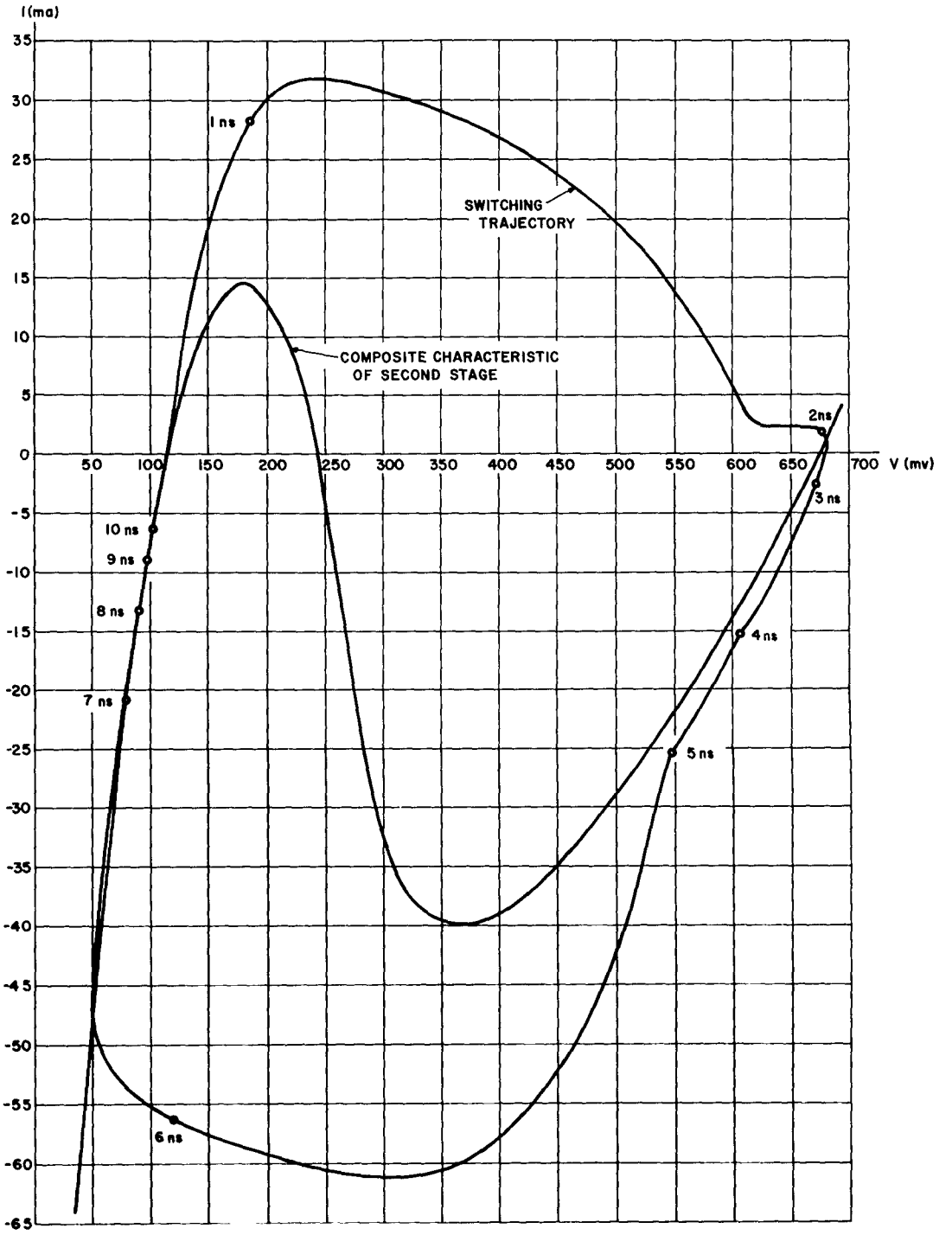


Figure 5-16. Switching Trajectory of Second Stage, Nominal Case

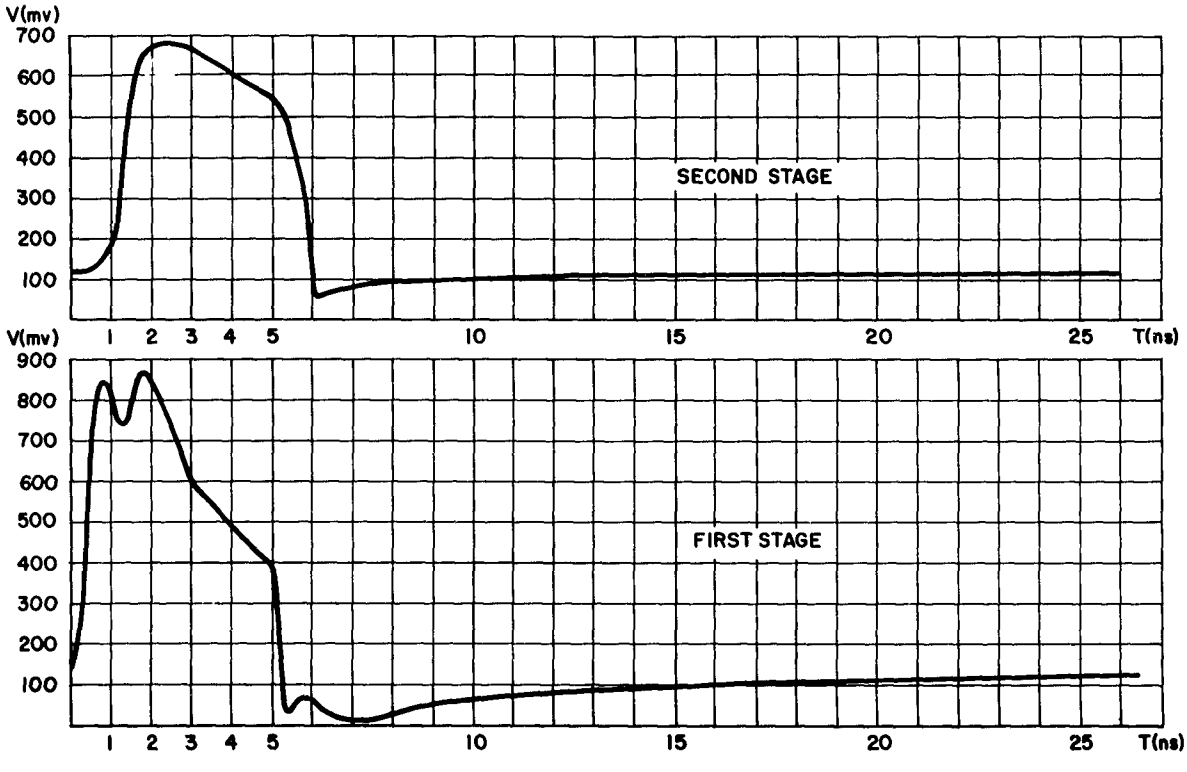


Figure 5-17. Digit Driver Outputs, Nominal Case

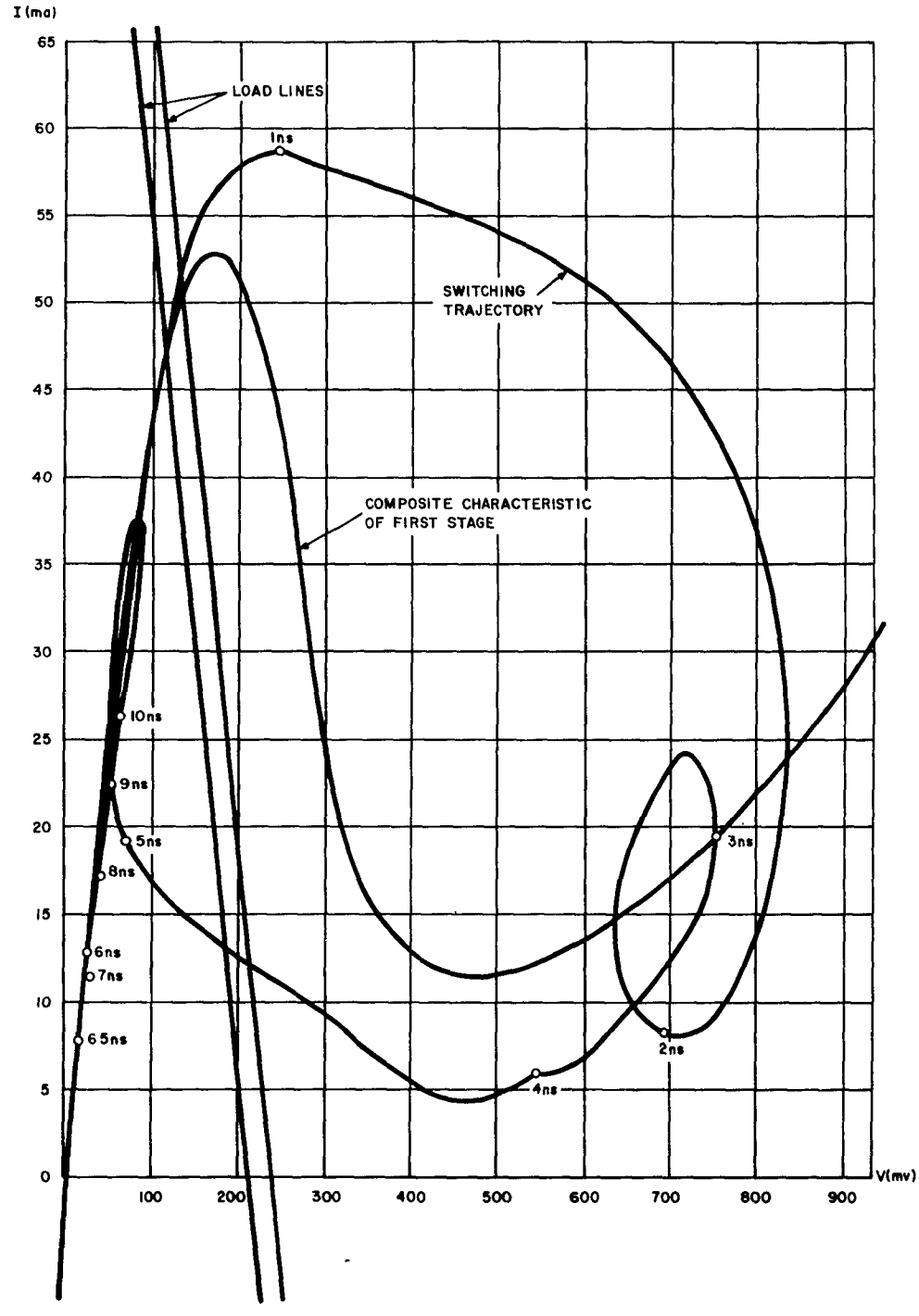


Figure 5-18. Switching Trajectory of First Stage, Worst-Case Switching

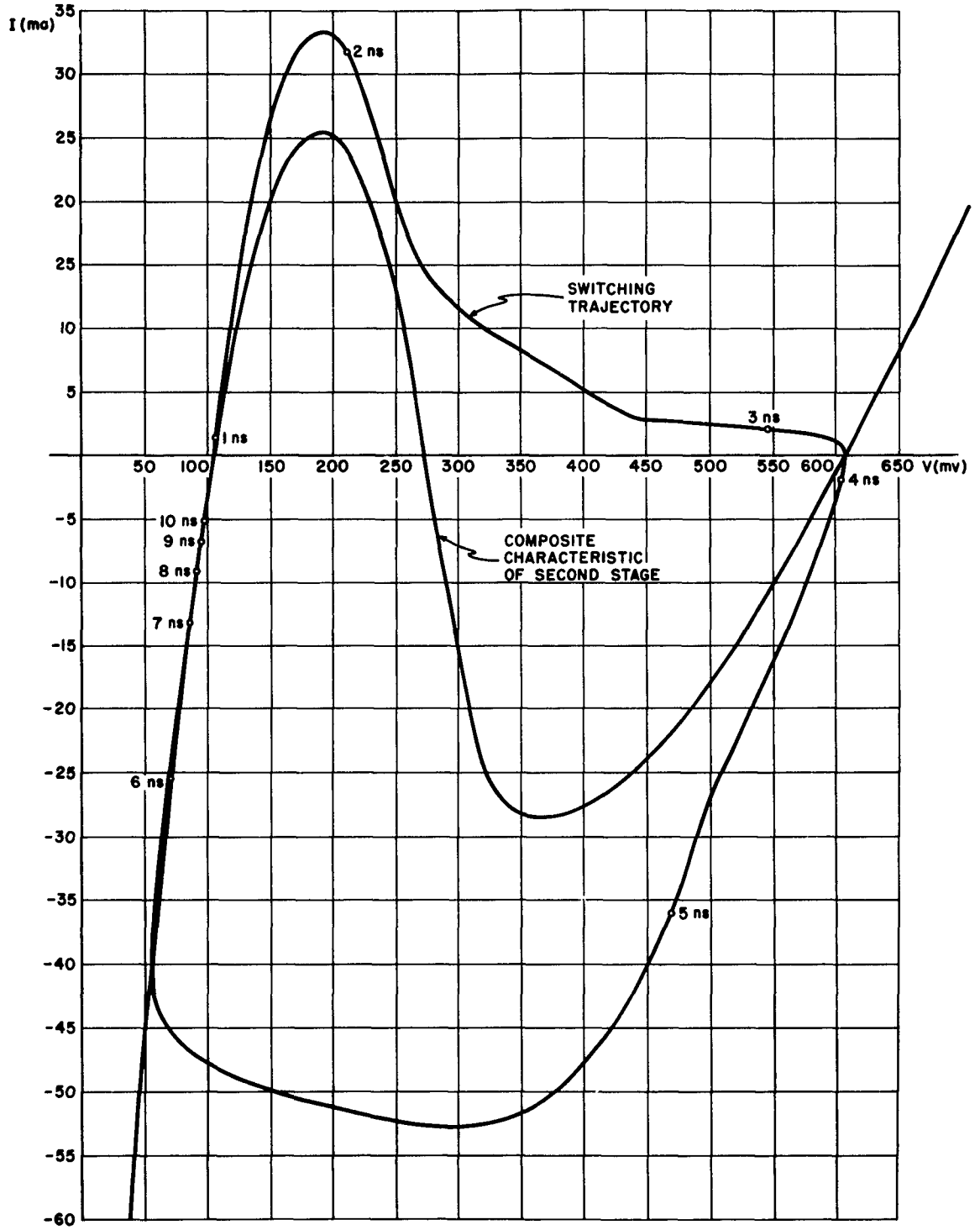


Figure 5-19. Switching Trajectory of Second Stage, Worst-Case Switching

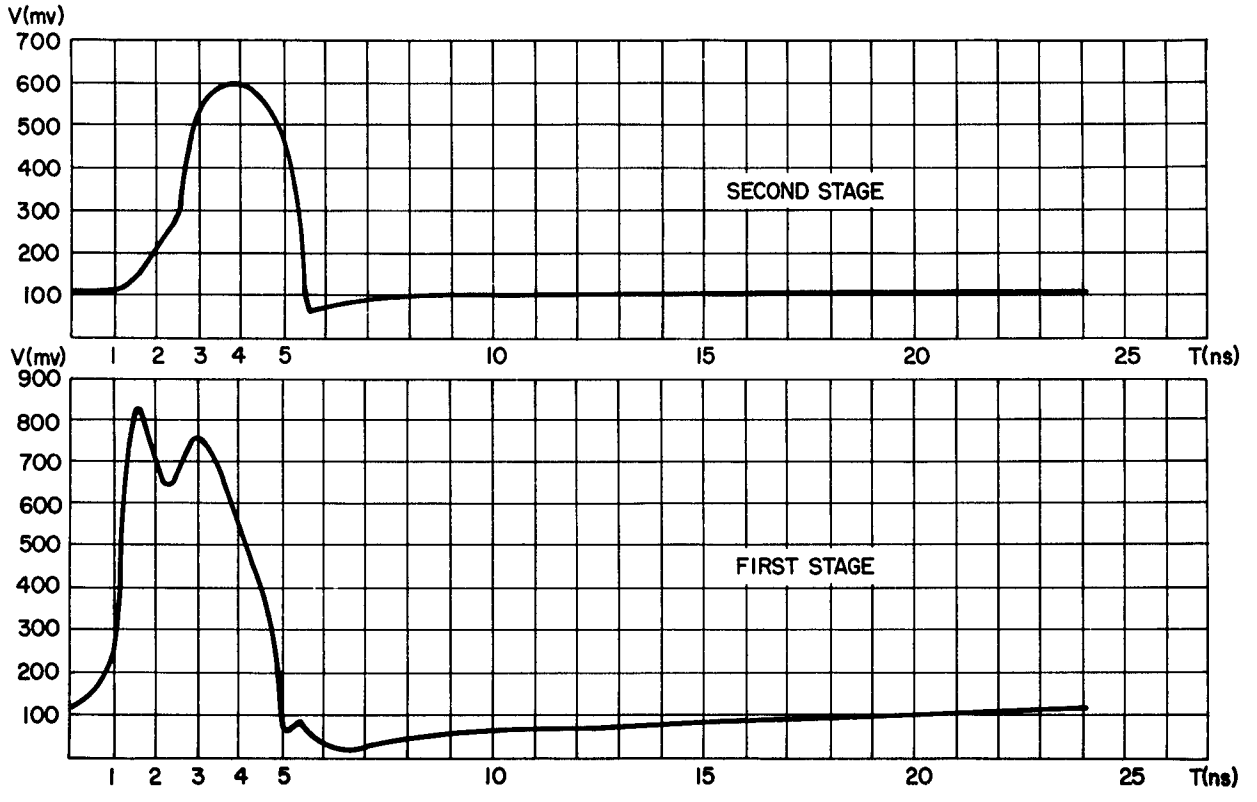


Figure 5-20. Digit Driver Outputs, Worst-Case Switching

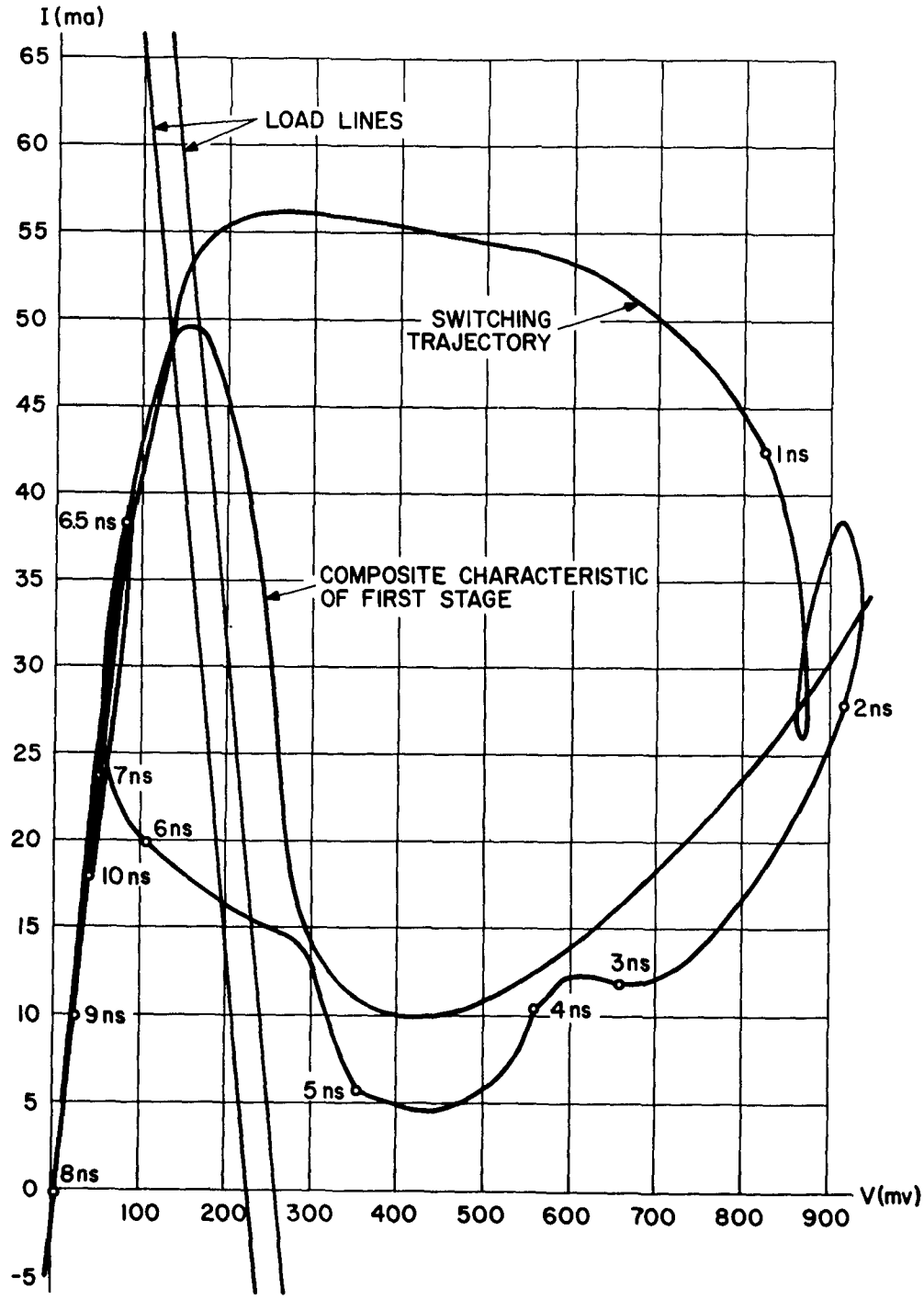


Figure 5-21. Switching Trajectory of First Stage, Worst-Case Resetting

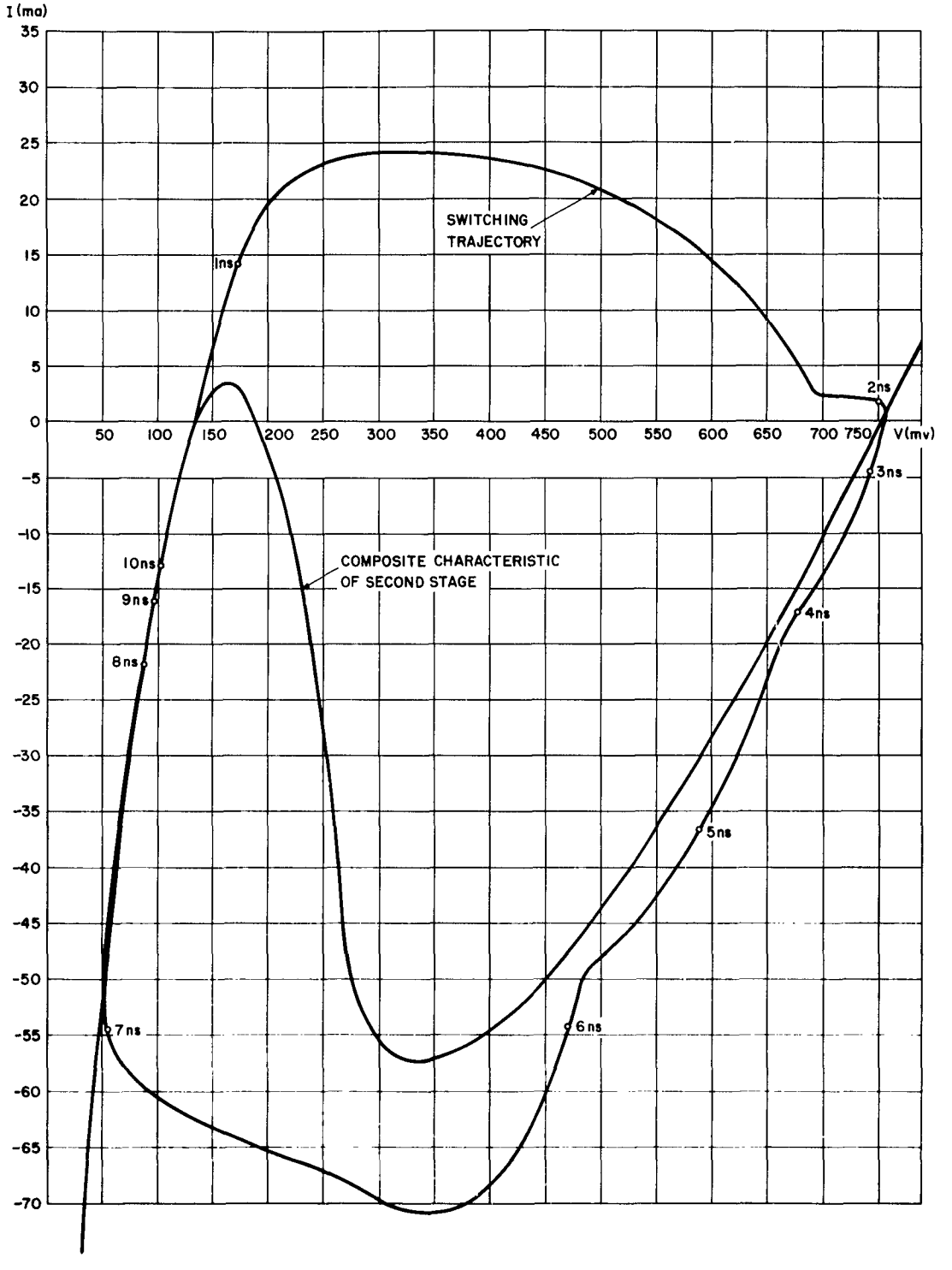


Figure 5-22. Switching Trajectory of Second Stage, Worst-Case Resetting

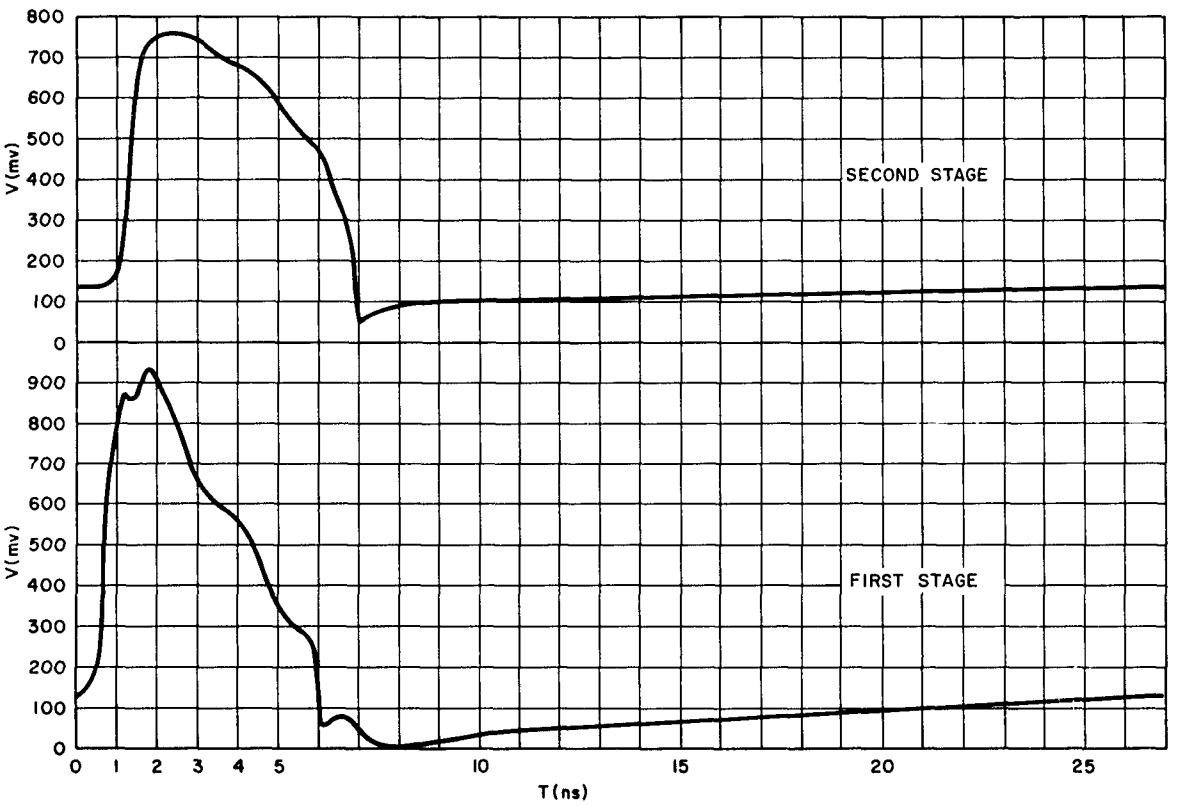


Figure 5-23. Digit Driver Outputs, Worst-Case Resetting

TABLE 5-3
TOLERANCES OF DIGIT DRIVER OUTPUTS

	Nominal Case	Worst-Case Switching	Worst-Case Resetting
Rise Time (ns)	0.7	1.41	0.56
Fall Time (ns)	0.47	0.37	1.12
Pulse Width (ns)	4.46	2.79	5.22
Period (ns)	26	24	27
V peak-V quiescent (mv)	566	503.5	627
Tilt (%)	26.8	33.8	32.6

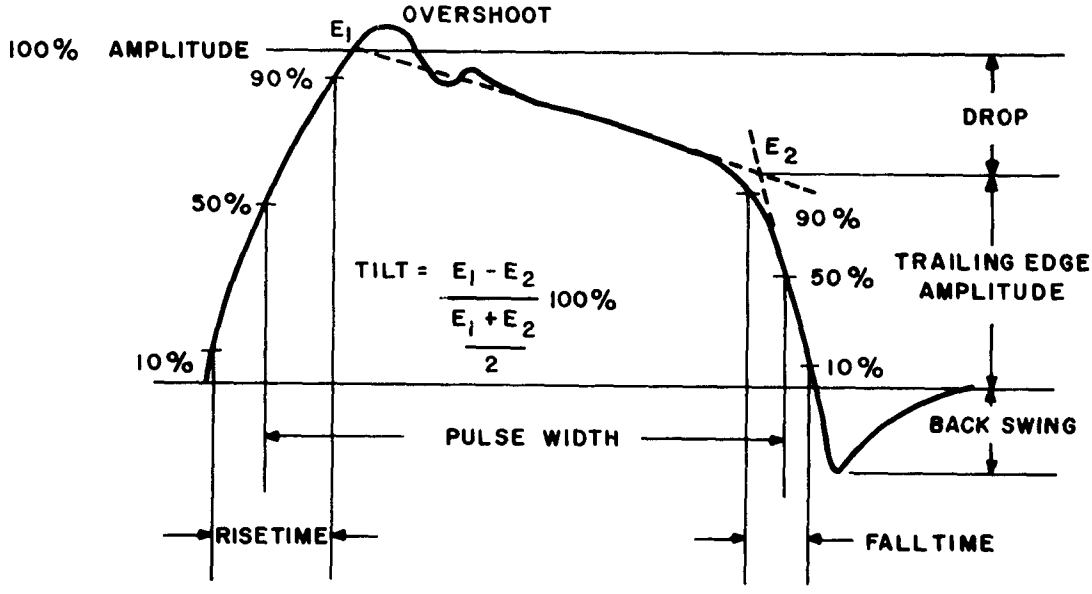


Figure 5-24. Pulse Waveform Details

E. SENSE AMPLIFIER

1. General

The nine- and 32-word memory subsystems require a sense amplifier to detect the output of the memory cell, which has a magnitude of approximately 35 mv, and can supply an input to the digit driver. A further requirement of the sense amplifier is that it appear as a termination at the end of the digit line. A dynamic study of the sense amplifier circuit was made to determine its operation and to define its circuit parameters under worst-case conditions. The dynamic study was made using the graphical method described in IRR-10A. In addition to the graphical method, study of the circuit on a digital computer is presently underway. This additional study will optimize circuit values and provide results more rapidly than is possible graphically.

A second stage for the sense amplifier has been designed and analyzed statically. The circuit, shown in Figure 5-25, gives the values presently being considered. Some adjustment will be made in inductance values to obtain optimum operation.

2. Dynamic Study

A dynamic study using the graphical method was made on the simplified equivalent circuit, Figure 5-26. Initial conditions of the circuit were those determined by static considerations of worst case for switching. Tolerance on all resistors was ±2% and voltage supplies ±2%. Tunnel diodes D_1 and D_2 had tolerances of ±2% on I_p and ±5% on E_p. Maximum capacity of D_1 and D_2 was taken as 3.5 pf.

Switching trajectories were plotted with the above conditions. The input was assumed to be a step of current of 1.5 ma in amplitude having a duration of 2 ns. A critical portion of its switching trajectory occurred after D_1 had switched over its peak and was in its negative-resistance region. L_1 and L_2 had to be large enough to keep sufficient current flowing in D_1 to insure that it switched into its valley region; otherwise, D_2 would not switch and very little output would be obtained. A second critical area occurred on recovery after the two diodes had switched back to their low state. Differences in the time constants of L_2 and D_1 and L_2 and D_2 resulted in a current buildup in D_1 which was faster than that in D_2. This caused the current in D_1 to overshoot its quiescent operating point by approximately 0.25 ma. Under conditions which would be the best case for switching, the circuit would tend to switch again unless this overshoot were eliminated or taken into account by lowering the quiescent operating point. Figure 5-27 shows the switching trajectories of D_1 and D_2. From these trajectories, the output voltage waveforms and D_2 are derived as shown in Figure 5-28. Recovery time of the circuit was found to be approximately 5 ns. Recovery time is sufficiently short to permit operation with the 25-ns cycle, since up to 15 ns can be allowed for recovery. The output voltage was only 350 mv which could be increased by increasing the value of L_2. Recovery time could be increased but could only be tolerated to the extent indicated above.

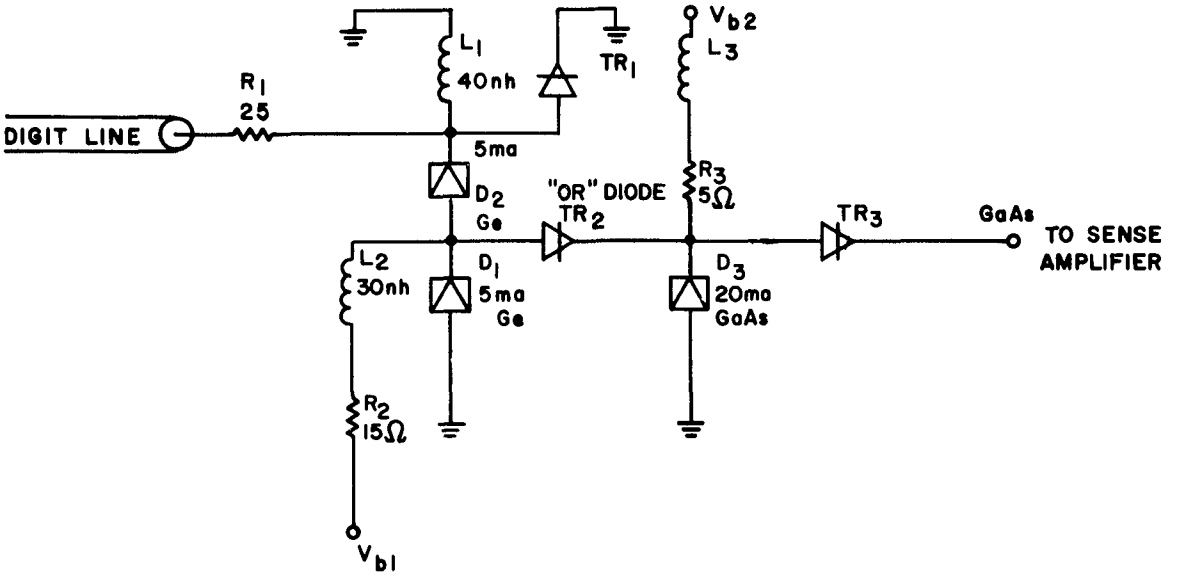


Figure 5-25. Sense Amplifier Circuit

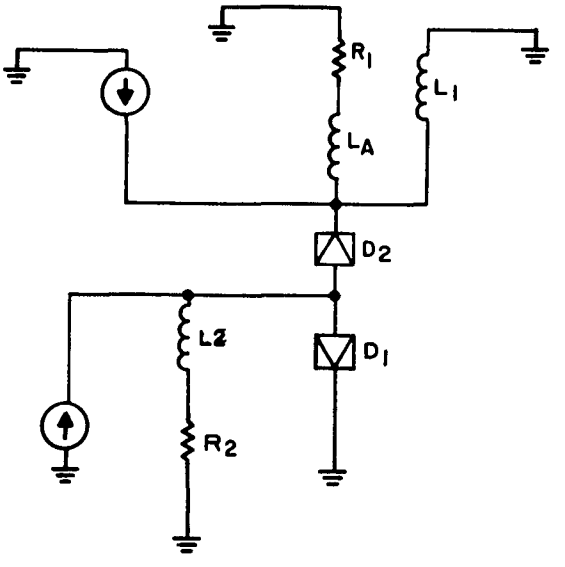


Figure 5-26. Simplified Equivalent Sense Amplifier Circuit

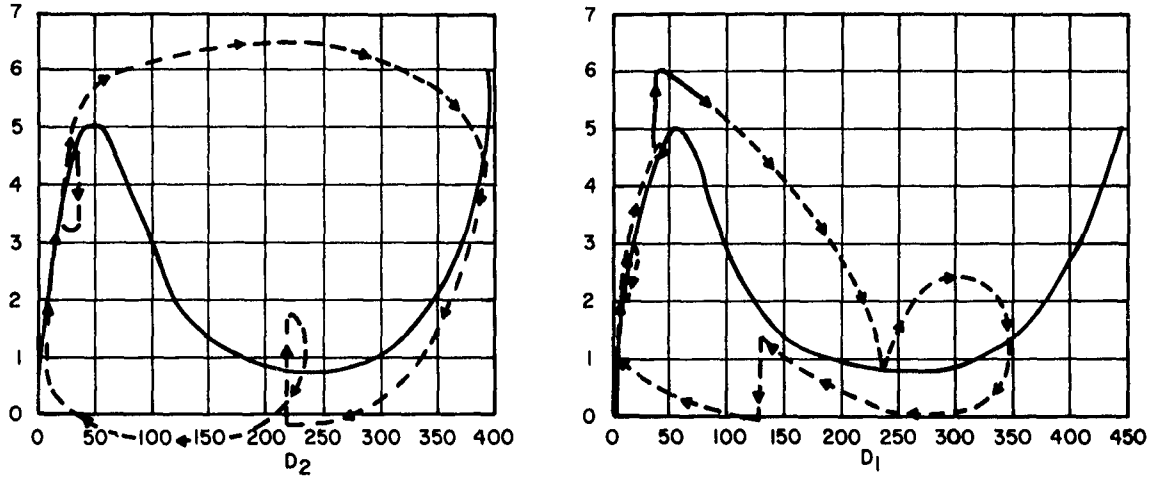


Figure 5-27. Sense Amplifier Switching Trajectories

This analysis, while closely approximating circuit conditions during switching, became invalid after the circuit switched because TR_3 then conducts. It was desired in this analysis to determine whether the circuit would switch under operating condition and whether it would recover sufficiently fast. Results of the computer study will give a more exact solution.

3. Second Stage

The sense amplifier must supply an output to the digit driver of approximately 15.6 ma while not interfering with its operation after it has switched. Because of the large voltage swing associated with the digit driver, TR_3 must be a GaAs rectifier to prevent loading. It is also desirable to use a GaAs tunnel diode in order that specifications on the forward dynamic resistance of TR_3 do not become severe. Coupling between stages of the sense amplifier is accomplished by an OR diode which has 1 pf maximum capacity and thereby does not load the first stage where tolerances are very tight. The result of static analysis indicate a 20-ma diode will be satisfactory. The dynamic study will have to be completed before this circuit is finalized.

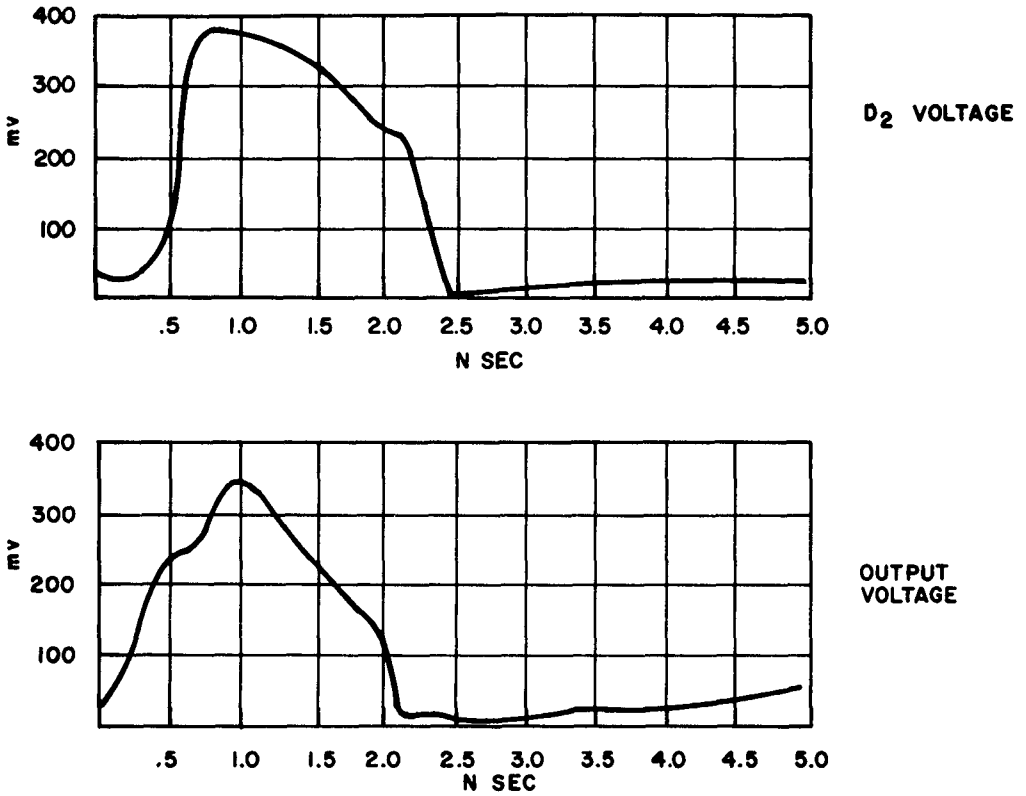


Figure 5-28. Sense Amplifier Waveforms

F. GENERAL SYSTEM LABORATORY RESULTS

The second plane in the nine-word system was added and successful regeneration of all 18 bits was obtained. The maximum repetition rate in the regeneration loop is 43 mc. The word read and write time was 12 ns in the 1st plane; however, in the 2nd plane it is 10 ns. In spite of the shorter word read and write time, the coincidence of the digit and word write pulse was still sufficient for regeneration of the cells in

the 2nd plane. The 5-ma Ge tunnel diodes used in the 2nd plane memory cells were picked to meet the following specifications:

I_p = 5 ma ±5%

E_p = 70 mv ±5%

E_x = 475 mv ±5%

C ≤ 10 pf

The tunnel rectifier specifications for the 2nd plane is E_r (at-4ma) ≤ -225 mv; 1050 mv ≤ E_f (at 1 ma) ≤ 1150 mv; and C ≤ 3.5 pf.

The tunnel rectifiers used in the 1st plane had the following specifications: E_r (at -4ma) ≤ -225 mv; 950 mv ≤ E_f (at 1 ma) ≤ 1050 mv; and C ≤ 3.7 pf.

The above specifications represents a ±10% tolerance on E_f.

Since the peak voltages of the 250-ma tunnel diodes of the word drivers vary by approximately ±20% around 275 mv, a separate bias source was connected to the word line to obtain zero volts on the word line.

Figure 5-29 shows that the maximum repetition rate is 50 mc for the first word driver in the 1st plane. No other word drivers were activated for this test.

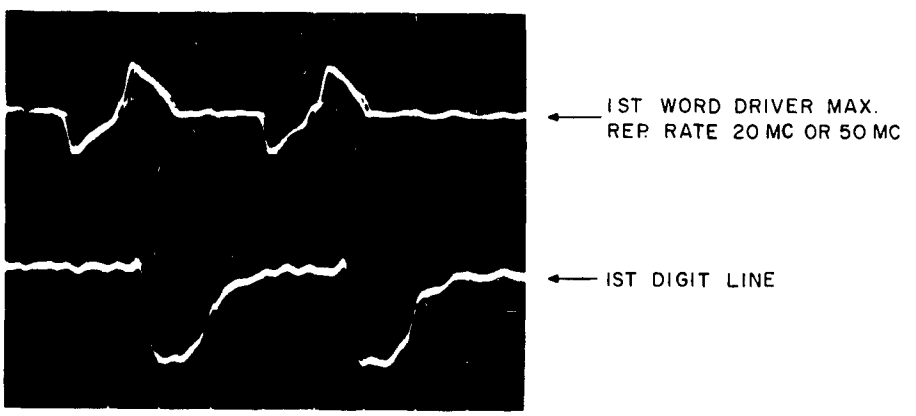


Figure 5-29. Word Driver and Digit Line Waveforms

III. PROGRAM FOR NEXT INTERVAL

All 27 memory cells of the nine-word system will be made operable.

Work will continue on the 32-word, five-bit system. More specifically, the following will be completed:

Peripheral circuitry fabrication techniques

Computer Simulation of individual circuits

Fabrication of all planes.

Also, the first plane of the 32-word, five-bit system will be tested.

Chapter 6. SYSTEM STUDIES

Chapter 6. SYSTEM STUDIES

I. PERSONNEL

The following personnel contributed to this phase of the project during the eleventh quarter:

J. F. Page
M. J. Sendrow
P. Warburton

II. SUMMARY

A detailed discussion of the current systems work is contained in Appendix II of this report, entitled: "System Study Report Number 7". (This Appendix is published under separate cover for convenience of distribution.)

The table of contents of this report is:

The summary and figures are reprinted below:

This Appendix details the design of a computing system proposed under different assumptions from the ones previously proposed under this title. The structure of the machine is outlined; the registers, sequencing, addressing, instruction repertoire, and the elaborate input-output system are described. Many questions of detail remain to be worked out.

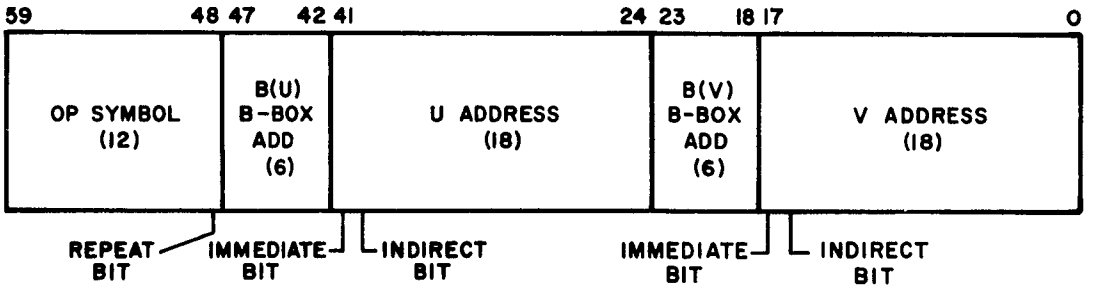


Figure 6-1. Instruction Word

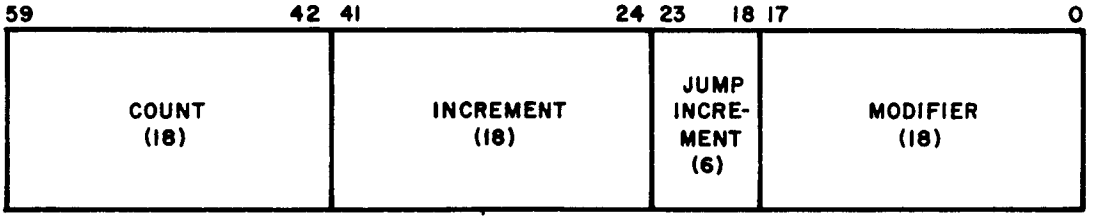
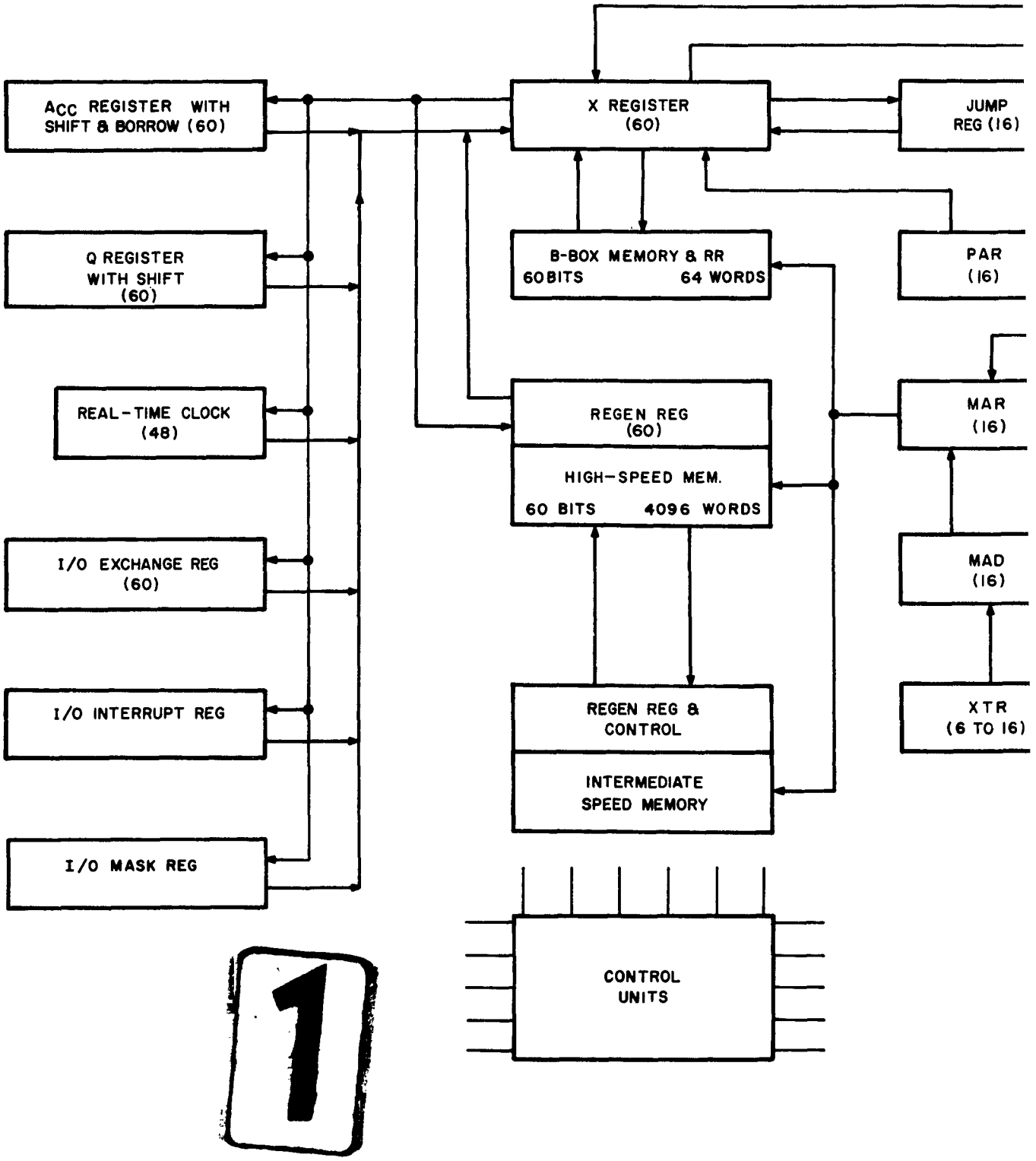


Figure 6-2. B-Box Word


ACC REGISTER WITH SHIFT & BORROW (60)
X REGISTER (60)
JUMP REG (16)
Q REGISTER WITH SHIFT (60)
B-BOX MEMORY & RR
60 BITS
64 WORDS
PAR (16)
REAL-TIME CLOCK (48)
REGEN REG (60)
HIGH-SPEED MEM.
60 BITS
4096 WORDS
MAR (16)
I/O EXCHANGE REG (60)
MAD (16)
I/O INTERRUPT REG
REGEN REG & CONTROL
INTERMEDIATE SPEED MEMORY
XTR (6 TO 16)
I/O MASK REG
CONTROL UNITS
1

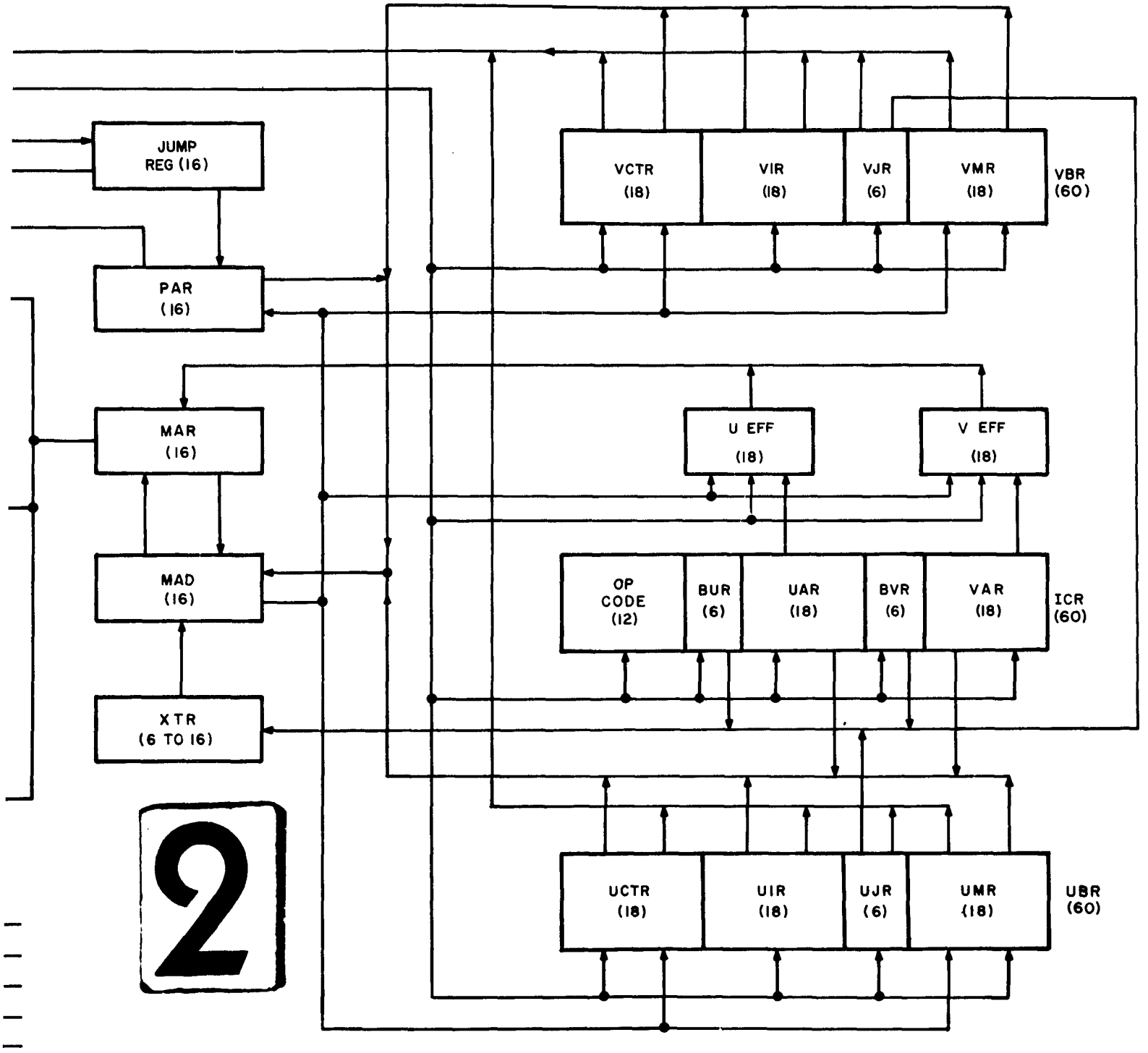
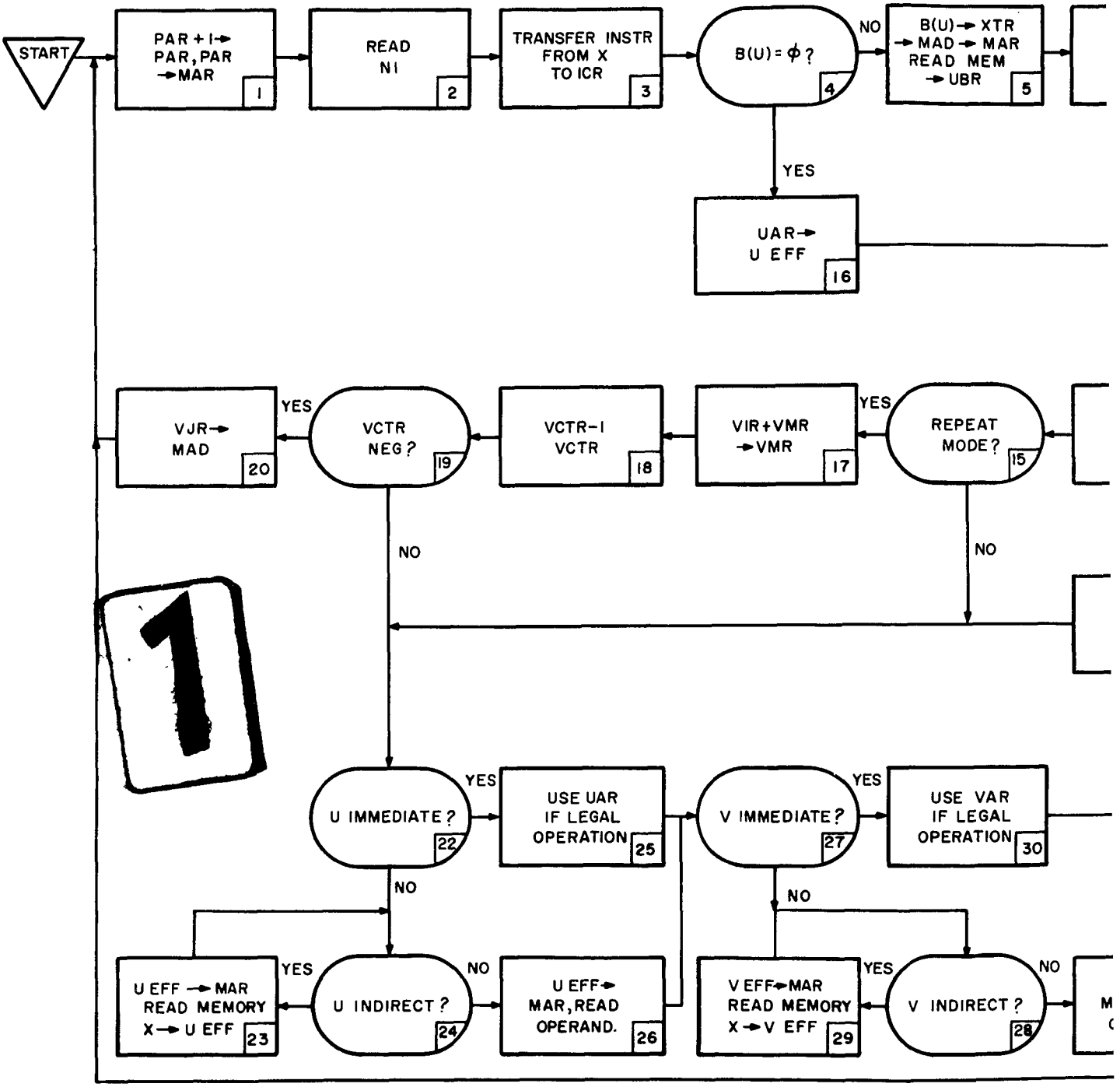


Figure 6-3. Control Registers, Minotaur I


START
PAR + 1 → PAR, PAR → MAR
1
READ N1
2
TRANSFER INSTR FROM X TO ICR
3
B(U) = ϕ ?
4
NO
B(U) → XTR → MAD → MAR READ MEM → UBR
5
YES
UAR → U EFF
16
VJR → MAD
20
YES
VCTR NEG?
19
VCTR - 1 VCTR
18
VIR + VMR → VMR
17
YES
REPEAT MODE?
15
NO
NO
1
U IMMEDIATE?
22
YES
USE UAR IF LEGAL OPERATION
25
V IMMEDIATE?
27
YES
USE VAR IF LEGAL OPERATION
30
NO
NO
U EFF → MAR READ MEMORY X → U EFF
23
YES
U INDIRECT?
24
NO
U EFF → MAR, READ OPERAND.
26
V EFF → MAR READ MEMORY X → V EFF
29
YES
V INDIRECT?
28
NO

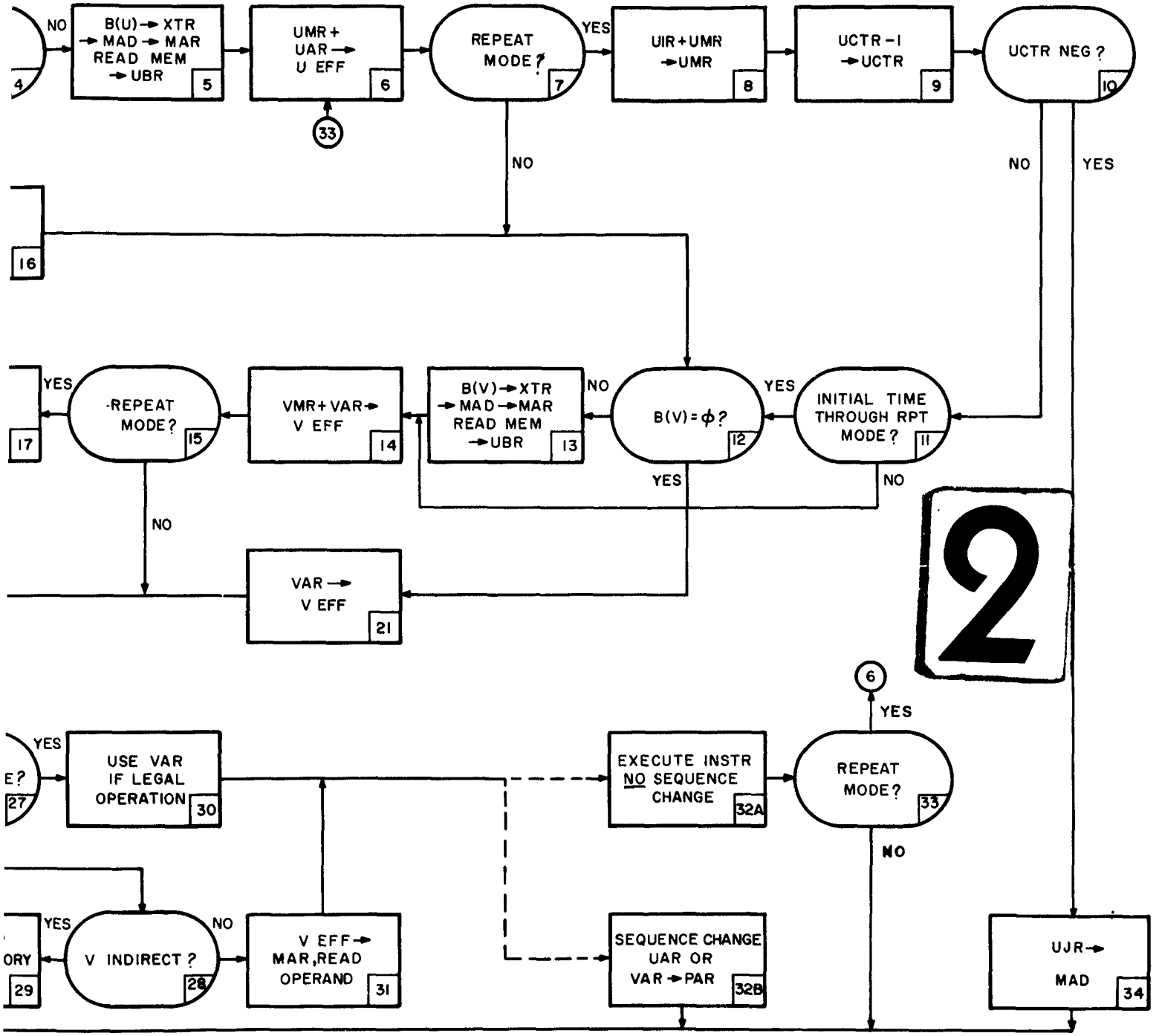


Figure 6-4. Euprosodopoesis — Minotaur I

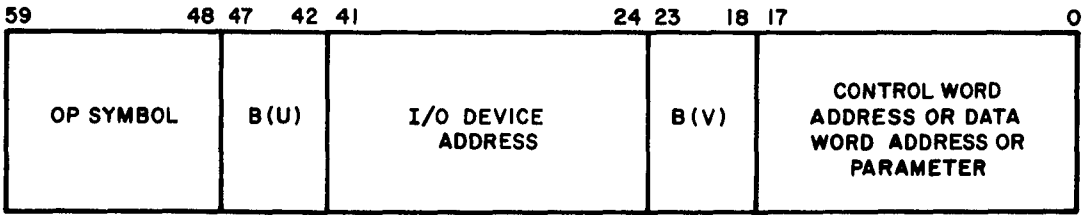


Figure 6-5. Input-Output Instruction Word

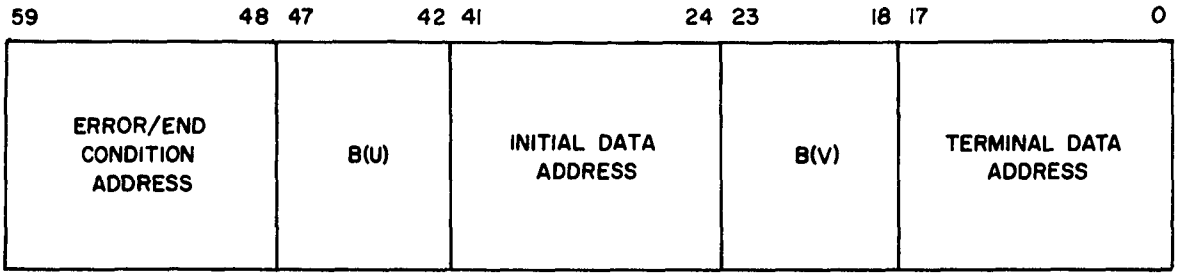


Figure 6-6. Initial I/O Control Word

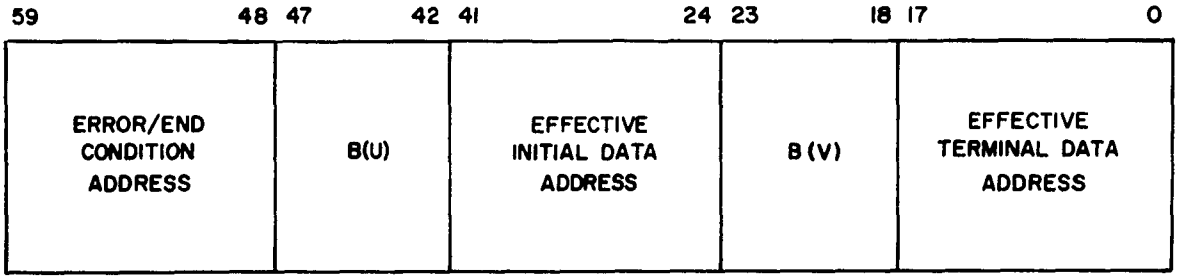


Figure 6-7. I O Control Word as Stored in Standard Location

APPENDIX I

DERIVATION OF A GENERAL, DIGITAL-COMPUTER PROGRAM FOR THE SOLUTION OF NON-LINEAR CIRCUITS

by H. R. Kaupp

The purpose of this report is to indicate a method of solving circuits containing solid-state tunneling devices without writing a new program for each specific circuit configuration to be analyzed. It is not the purpose here to present a detailed flow chart suitable for direct machine coding. The actual coding will depend not only on the machine to be used, but also on whether the coding is to be written in machine language or a meta-language, such as, ALGOL or FORTRAN.

Although the program is derived with tunnel diodes and tunnel rectifiers in mind, it can be modified to handle other non-linear elements. As written, the program is readily adaptable to linear circuits by suitably removing the non-linear elements. It is also practical for evaluating lumped transmission lines having linear or non-linear terminations.

Specific circuits are solved by mapping their schematic diagram on a general circuit. A biplanar circuit matrix, as shown in Figure I-1 is assumed. Each branch contains a mathematical model of a tunnel diode. The same model represents a tunnel rectifier; however, the "forward" direction of a tunnel diode is opposite of that of a tunnel rectifier. Each node of the general circuit is supplied with a current source and an associated resistance. This source can be used as a d-c bias or a driving signal of arbitrary waveform. If the circuit to be analyzed uses voltage rather than current sources, a simple Thevenin to Norton transformation readily adapts the source to the general circuit.

Using the notation indicated in Figure I-2, the equations that define an arbitrary branch and one of its associated nodes can be written as:

$$\frac{dV_{xy}}{dt} = \frac{1}{C_{xy}} \left[A_{xy} I_{xy} - B_{xy} I_{Dxy} \right] \tag{1}$$

$$\frac{dI_{xy}}{dt} = \frac{1}{L_{xy}} \left[V_x - V_y - A_{xy} V_{xy} - R_{xy} I_{xy} \right] \tag{2}$$

$$V_x = R_{gx} \left[I_x(T) + I_{p,q-1;pq} + I_{p-1,q;pq} - I_{pq;p,q+1} - I_{pq;p+1,q} \right] \tag{3}$$

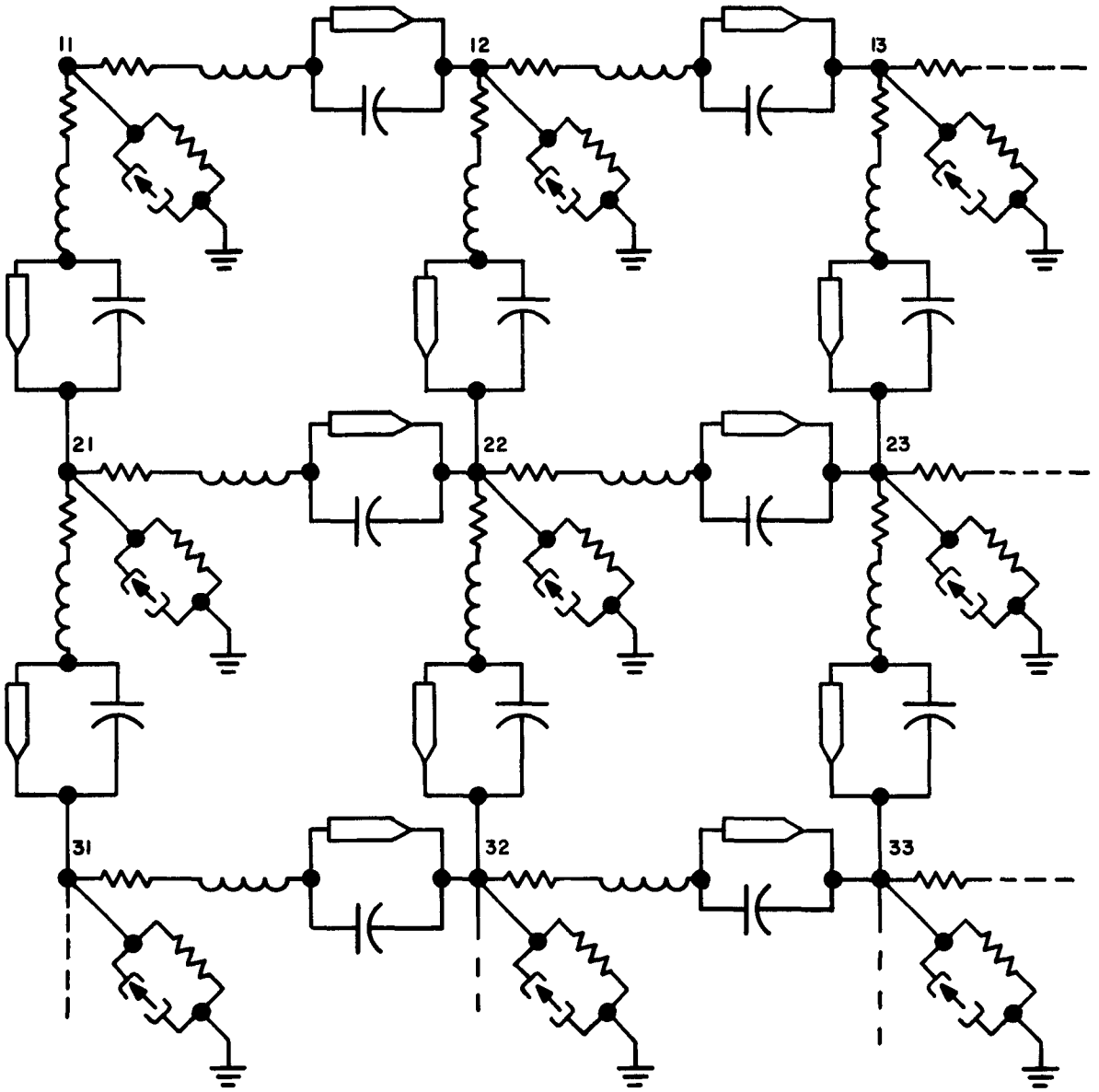


Figure I-1. General Map for the Solution of Tunnel Diode Circuits

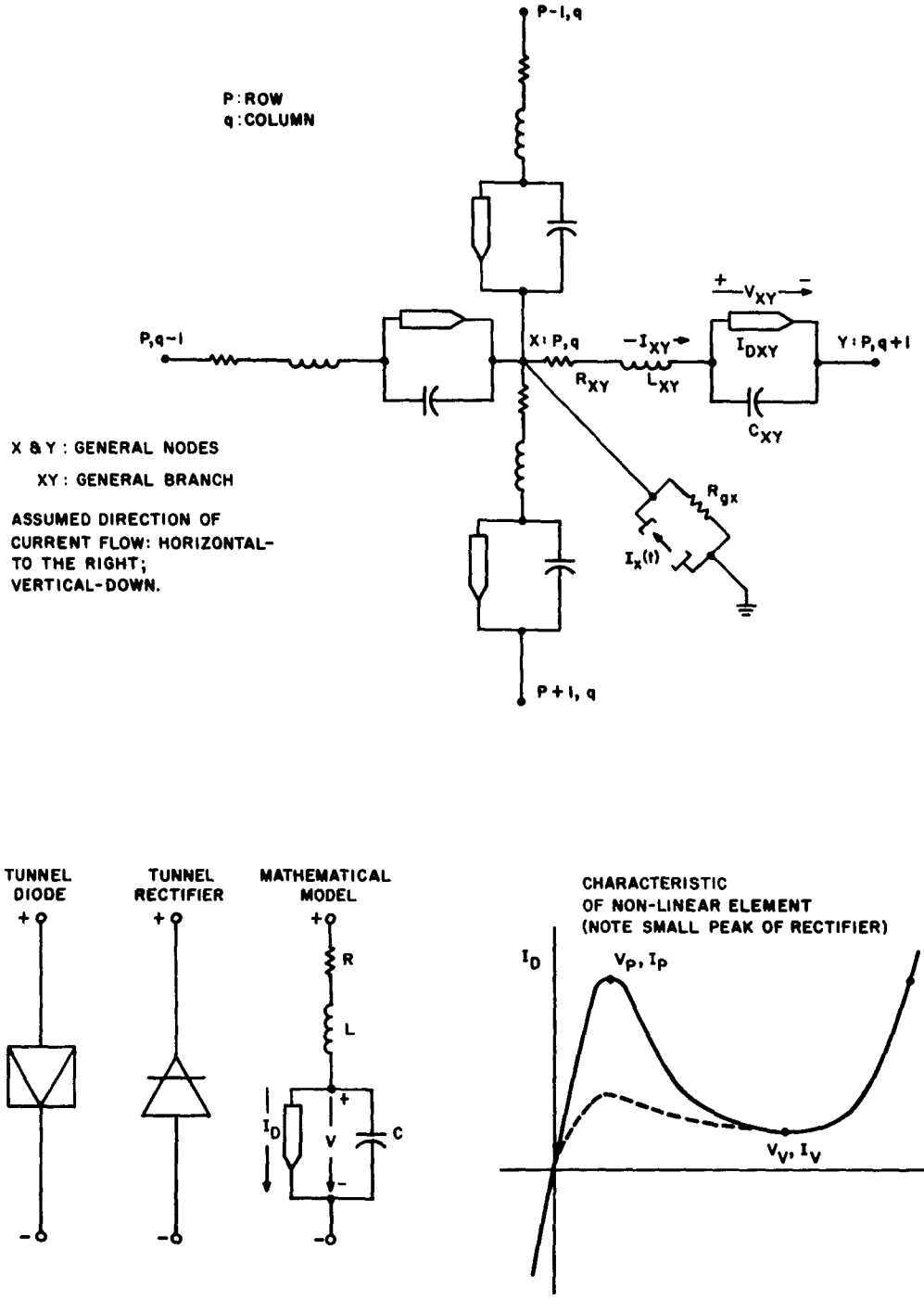


Figure I-2. Notation Specification

where A and B are control parameters whose function will be explained later. The analytic expression[1] used to represent the non-linear tunnel diode characteristic is:

$$I_{Dxy} = K1_{xy}V_{xy} + K2_{xy}V_{xy}^2 + K3_{xy}V_{xy}\, e^{\frac{2}{3}\left(\frac{V_{xy}}{V_{pxy}}\right)^{\frac{3}{2}}} + K4_{xy}\left[e^{K5_{xy}V_{xy}} - 1\right] \tag{4}$$

The constants K1 through K5 can be calculated in a separate subroutine, given at least five restraining coordinates of the tunnel diode I-V curve (Figure I-2). Since each branch in the general circuit can be defined by a second order differential equation, two initial conditions must be specified for each branch. The reader will recall that to determine a numerical solution to a differential equation of second order, the equation is broken down into two simultaneous equations. Equations (1) and (2) are used here; thus, sufficient initial conditions are V_{xy} (o) and I_{xy} (o) (for all xy).

For illustrative purposes, a specific circuit configuration is shown in Figure I-3. The equations defining the circuit of this Figure are;

$$\frac{dV_{11,12}}{dt} = \frac{1}{C_{11,12}}\left[A_{11,12}I_{11,12} - B_{11,12}I_{D11,12}\right] \tag{11a}$$

$$\frac{dI_{11,12}}{dt} = \frac{1}{L_{11,12}}\left[V_{11} - V_{12} - A_{11}V_{11,12} - R_{11,12}I_{11,12}\right] \tag{11b}$$

$$\frac{dV_{11,21}}{dt} = \frac{1}{C_{11,21}}\left[A_{11,21}I_{11,21} - B_{11,21}I_{D11,21}\right] \tag{11c}$$

$$\frac{dI_{11,21}}{dt} = \frac{1}{L_{11,21}}\left[V_{11} - V_{21} - A_{11,21}V_{11,21} - R_{11,21}I_{11,21}\right] \tag{11d}$$

$$V_{11} = R_{11}\left[I_{11}(t) - I_{11,12} - I_{11,21}\right] \tag{11e}$$

$$\frac{dV_{12,22}}{dt} = \frac{1}{C_{12,22}}\left[A_{12,22}I_{12,22} - B_{12,22}I_{D12,22}\right] \tag{12a}$$

$$\frac{dI_{12,22}}{dt} = \frac{1}{L_{12,22}} \left[V_{12} - V_{22} - A_{12,22}V_{12,22} - R_{12,22}I_{12,22}\right] \quad (12b)$$

$$V_{12} = R_{12} \left[I_{12}(t) + I_{11,12} - I_{12,22}\right] \quad (12c)$$

$$\frac{dV_{21,22}}{dt} = \frac{1}{C_{21,22}} \left[A_{21,22}I_{21,22} - B_{21,22}I_{D21,22}\right] \quad (21a)$$

$$\frac{dI_{21,22}}{dt} = \frac{1}{L_{21,22}} \left[V_{21} - V_{22} - A_{21,22}V_{21,22} - R_{21,22}I_{21,22}\right] \quad (21b)$$

$$V_{21} = R_{21} \left[I_{11} + I_{11,21} - I_{21,22} - I_{21,31}\right] \quad (21c)$$

$$\frac{dV_{21,31}}{dt} = \frac{1}{C_{21,31}} \left[A_{21,31}I_{21,31} - B_{21,31}I_{D21,31}\right] \quad (21d)$$

$$\frac{dI_{21,31}}{dt} = \frac{1}{L_{21,31}} \left[V_{21} - V_{31} - A_{21,31}V_{21,31} - R_{21,31}I_{21,31}\right] \quad (21e)$$

$$\frac{dV_{22,23}}{dt} = \frac{1}{C_{22,23}} \left[A_{22,23}I_{22,23} - B_{22,23}I_{D22,23}\right] \quad (22a)$$

$$\frac{dI_{22,23}}{dt} = \frac{1}{L_{22,23}} \left[V_{22} - V_{23} - A_{22,23}V_{22,23} - R_{22,23}I_{22,23}\right] \quad (22b)$$

$$\frac{dV_{22,32}}{dt} = \frac{1}{C_{22,32}} \left[A_{22,32}I_{22,32} - B_{22,32}I_{D22,32}\right] \quad (22c)$$

$$\frac{dI_{22,32}}{dt} = \frac{1}{L_{22,32}} \left[V_{22} - V_{32} - A_{22,32}V_{22,32} - R_{22,32}I_{22,32}\right] \quad (22d)$$

$$V_{22} = R_{22} \left[I_{22} + I_{21,22} + I_{12,22} - I_{22,23} - I_{22,32}\right] \quad (22e)$$

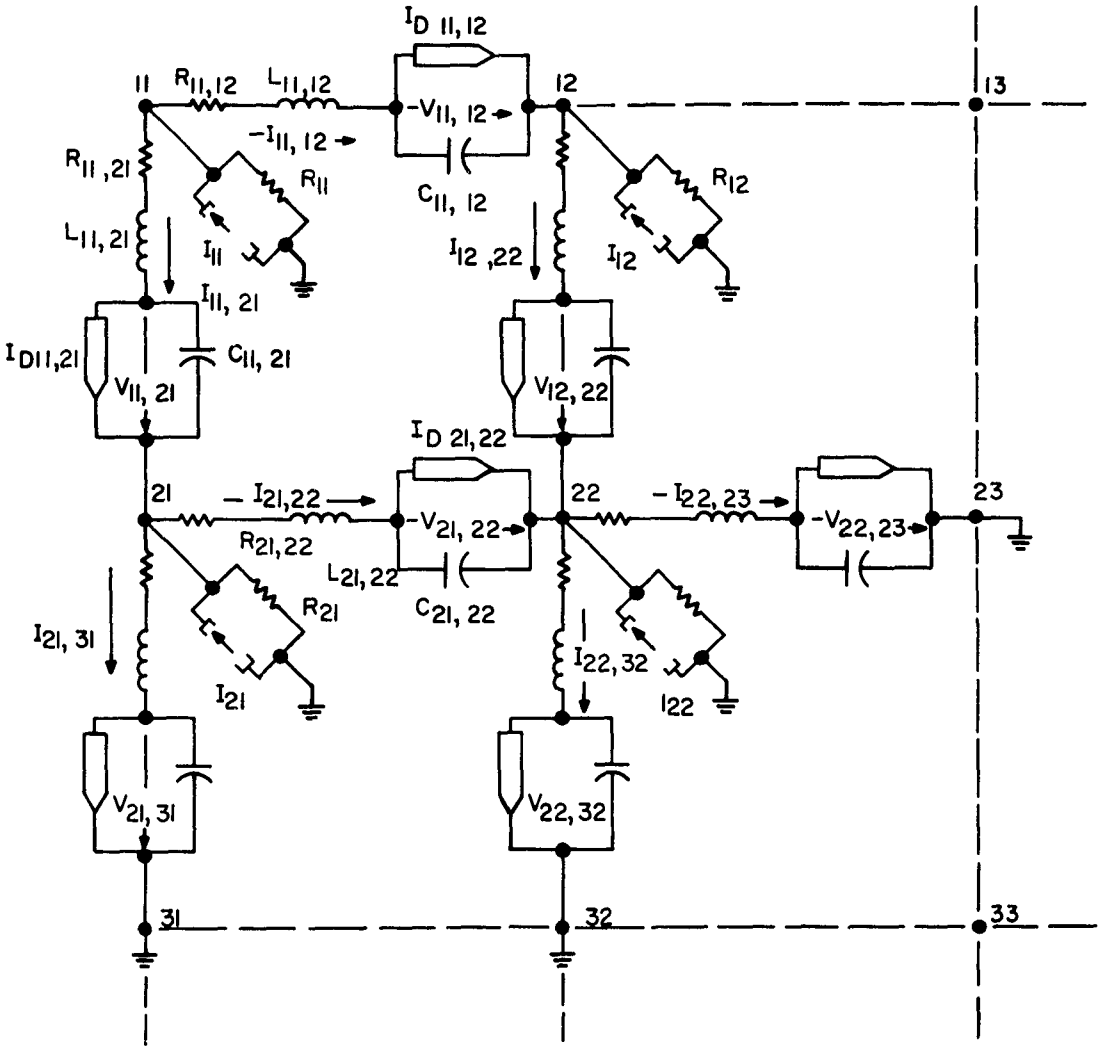


Figure I-3. Example of a Specific Circuit Mapped on the General Circuit

Henceforth, in the interest of clarity, the general circuit will be referred to as the general map; while a specific circuit, which is mapped on the general map, will be referred to as a sub-map. A rectangular sub-map is that sub-map defined by the maximum and minimum rows and columns of the general map that are used in the circuit sub-map. In addition, any node that does not appear on the circuit sub-map shall be known as an unspecified node. Referring to the circuit sub-map in Figure I-3, nodes 11, 13, 33, 31 define the rectangular sub-map and nodes 13 and 33 are unspecified.

Examining the general equation, (3), with regard to the sub-map in Figure I-3, it is seen that currents appear in this equation which are not defined in the sub-map. For instance, although there are no currents flowing horizontally from the left or vertically from above into node 11 on the sub-map, these currents are implicit in general equation (3). Therefore for any unspecified node, x, adjacent to a node, y, which is in the sub-map, it is necessary to set the current, I_{xy}, associated with these nodes equal to zero. Thus, undefined currents appearing in equation (3) are evaluated as being zero, which in fact they are. To facilitate this operation in the program, it is necessary to specify the rectangular sub-map of the specific circuit in the input data.

The function of control parameters A and B is to eliminate solving certain unnecessary equations. Consider open branches. An open branch is a branch that appears between two adjacent nodes (x and y), that are both in the sub-map, through which no current flows. An open branch is specified by setting control parameter A_{xy} equal to two. In this event, general equations (1) and (2) are not evaluated in the program. Furthermore, I_{xy} is set equal to zero thus defininig I_{xy} for its implicit appearance in equation (3).

A shorted branch is more difficult to obtain. This is true because a shorted branch implies six diode branches connected to one node instead of four. As written, the flow chart allows only one shorted branch per node. This restricts the program to solutions for circuits having no more than 6 diode branches connected to a node. The current source and its associated resistance can still be present, although only one of the two current sources connected through the shorted branch would be used.

A shorted branch is denoted by setting A_{xy} equal to minus two. If the branch xy is shorted, equation (3) is rearranged to solve for I_{xy}, the current in the shorted branch. Then the equation for V_y and I_{xy} are solved simultaneously. This is possible since $V_x = V_y$. Once again equations (1) and (2) are not evaluated.

In the example of Figure I-3 if branch 21, 22 is shorted, the equation of $I_{21,22}$ in terms of V_{22} is,

$$I_{21,22} = \frac{I_{21} + I_{11,21} - I_{21,31} - \frac{R_{22}}{R_{21}}\left[I_{22} + I_{12,22} - I_{22,23} - I_{22,32}\right]}{1 + \frac{R_{22}}{R_{21}}}$$

V_{22} is solved using equation (3). Equations (21a) and (21c) are not evaluated.

If more than one shorted branch per node is necessary, the additional shorted branch, xy, can be achieved by setting A_{xy} and R_{xy} equal to zero and letting L_{xy} be very small. Perhaps this is the most practical way to short a branch in the first place.

If in the general branch xy it is desirable to remove, or open circuit, the non-linear element while retaining its associated capacity, control parameter B_{xy} is set equal to zero. In this event, equation (4) is not evaluated. To short the non-linear element and its associated capacity, control parameter A_{xy} is set equal to zero. When A_{xy} equals zero, equation (1) is not evaluated.

If the direction of the non-linear element on the sub-map is opposite to the direction of its image on the general map, control parameter A is set to minus one. It should be noted from Figure I-2 that the forward direction of the tunnel rectifier and the tunnel diode are opposite in sense. Where the non-linear element appears in a branch and its direction is the same on the general map and sub-map, the control parameters A and B are set to one. The input specifications necessary to obtain particular branch configurations are summarized in Table I-1.

The inductance, L, and the source resistance, R_g, cannot be set to zero in this program. It would be best to use the reciprocal of these values and set them equal to infinity where necessary. In this event, infinity would be defined by some large number, such as 10^{30}.

The information that must be specified by the user of this program is as follows:

(1) Reference (grounded) Nodes — the voltage of a reference node is identically zero. For the example of Figure I-3, specify that 31, 32 and 23 are reference nodes and also that:

$$V_{31} = 0, \quad V_{32} = 0, \quad V_{23} = 0.$$

(2) Rectangular Sub-Map — in the example, nodes 11, 31, 33 and 13, define the rectangular sub-map.

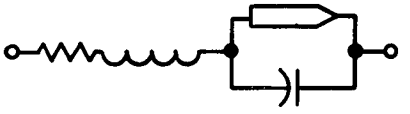
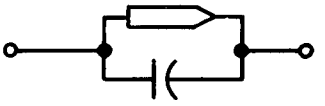
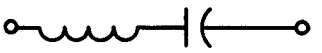
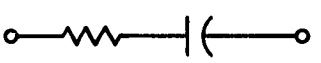
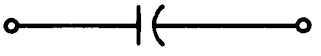
(3) Initial Conditions — V_{xy} (o) and I_{xy} (o) for all branches xy. It is not necessary to specify the initial current in a shorted branch.

(4) Restraining Coordinates of Non-Linear Element (Figure I-2) — five restraints are needed to evaluate the constants of equation (4). The three points indicated in Figure I-2, together with the derivative of I_D with respect to V evaluated at the peak and valley of the characteristic, yield the necessary equations.

The flow chart of Figure I-4 indicates that the topology of the specific circuit is evaluated on each pass through the routine. That is to say, the program looks to see if a branch or node is present before evaluating its associated equations. This is inefficient. It would be better if the circuit topology is evaluated on the first pass through the circuit matrix and then the indexing set in such a manner that the equations could be evaluated in sequence.

TABLE I-1

SPECIFICATION OF PARAMETERS FOR VARIOUS BRANCH CONFIGURATIONS

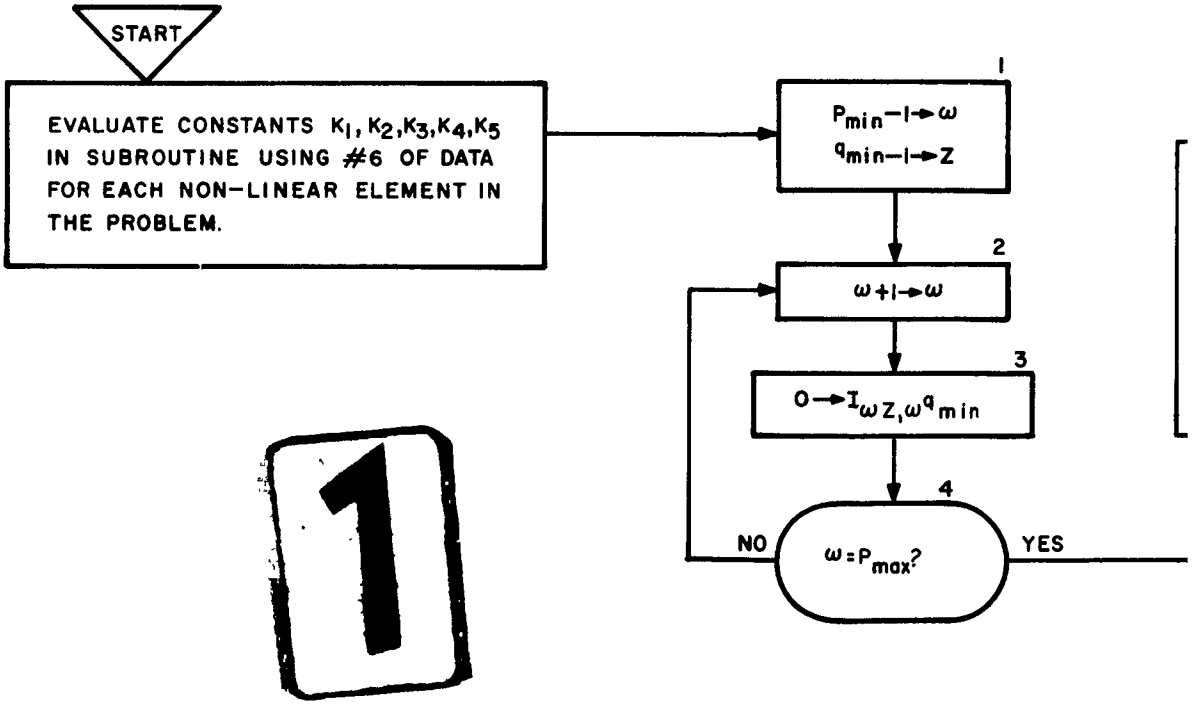
TYPE OF BRANCH	PARAMETER SPECIFICATION	
	A = 1 * B = 1	
	A = 1 * B = 1	1/L = ∞ R = 0
	A = 1 B = 0	
	A = 1 B = 0	R = 0
	A = 1 B = 0	1/L = ∞
	A = 1 B = 0	R = 0
	A = 0	
	A = 0	1/L = ∞
	A = 0	R = 0
OPEN BRANCH	A = 2	
SHORTED BRANCH	A = -2	

* OR −1 DEPENDING ON DIRECTION

$\infty \equiv 10^{30}$

READ IN DATA:

1. CIRCUIT PARAMETERS: R, L, C, R_g
2. DRIVING FUNCTIONS: $I_x(T)$
3. CONTROL PARAMETERS: A, B
4. INITIAL CONDITIONS: $V_{xy}(0), I_{xy}(0)$
5. DIMENSIONS OF CIRCUIT RECTANGULAR SUB-MAP: $P_{min}, P_{max}, q_{min}, q_{max}$
6. FIVE RESTRAINTS FOR EVALUATION OF NON-LINEAR ELEMENT CHARACTERISTIC
7. NUMBER OF NON-LINEAR ELEMENTS
8. REFERENCE (GROUNDED) NODES SPECIFIED AND VOLTAGES SET TO ZERO



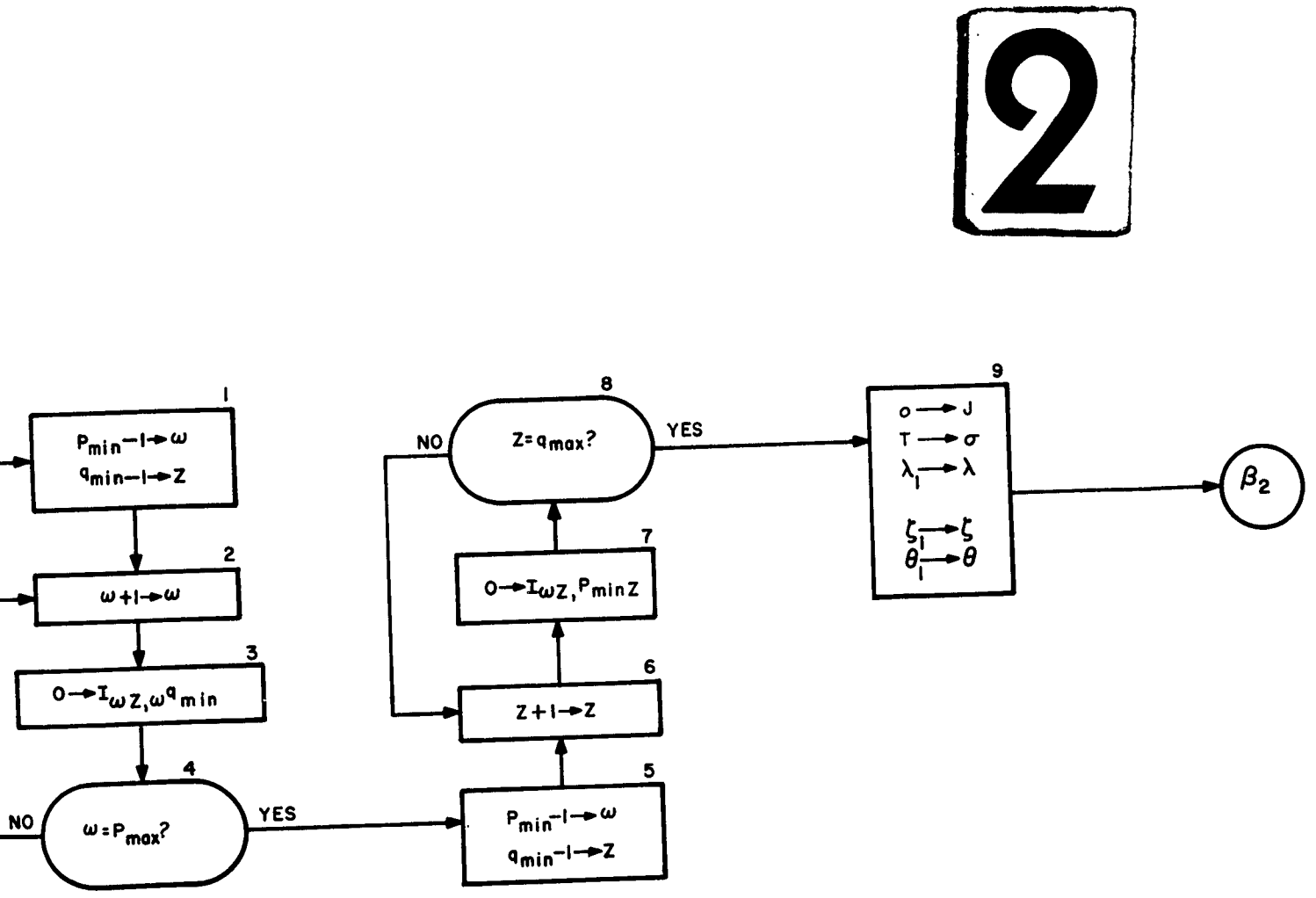
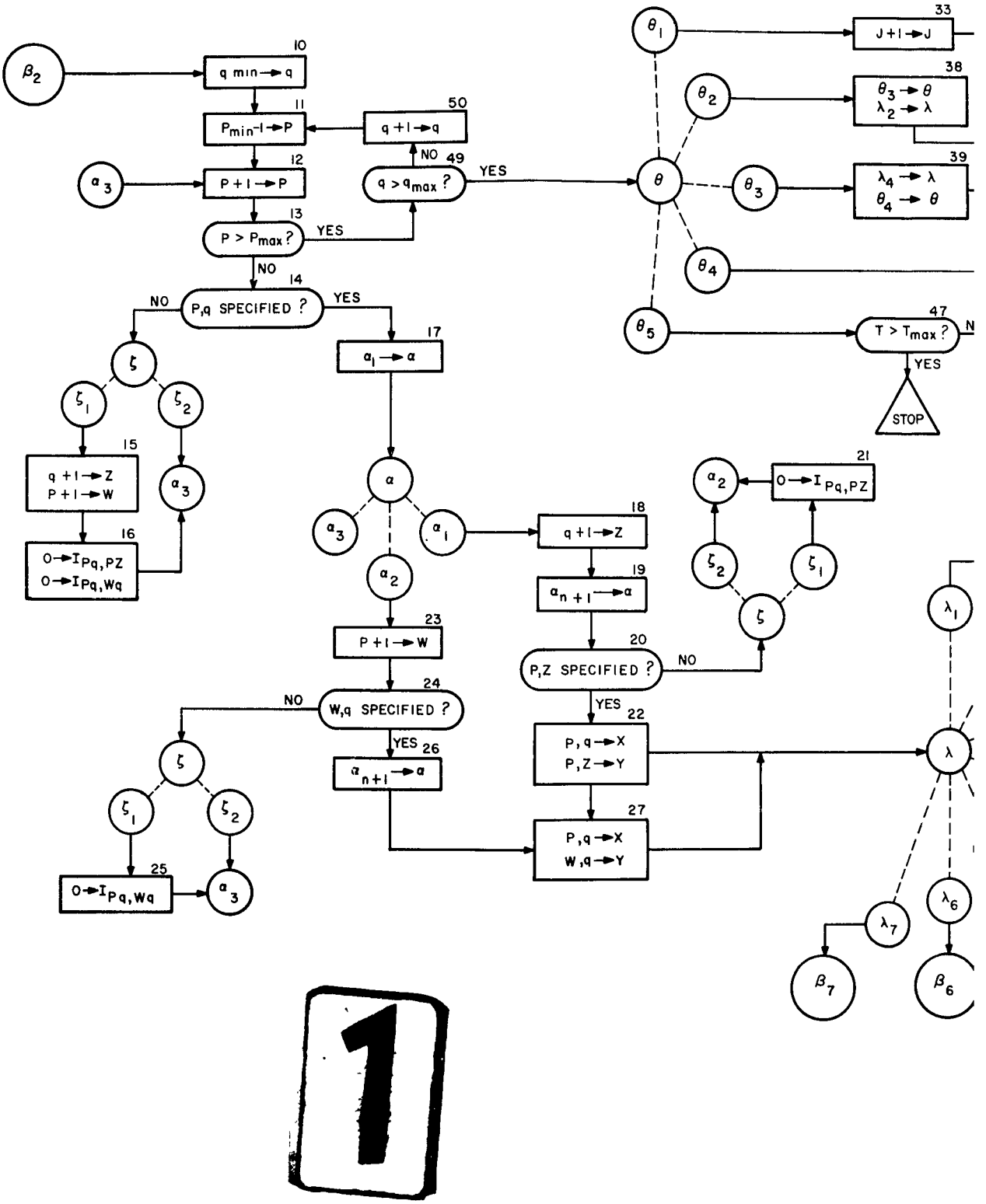


Figure I-4. *Flow Chart — General Program for Analysis of Linear or Non-Linear Circuit Problems using Fourth Order Runge-Kutta Method of Numerical Solution (sheet 1 of 3)*


β2
10
q min → q
11
Pmin−1 → P
50
q + 1 → q
12
P + 1 → P
α3
NO 49
q > qmax ?
YES
13
P > Pmax ?
YES
NO
14
P,q SPECIFIED ?
NO
YES
17
α1 → α
ζ
ζ1
ζ2
15
q + 1 → Z
P + 1 → W
α3
16
0 → IPq,PZ
0 → IPq,Wq
α
α3
α1
α2
18
q + 1 → Z
19
αn + 1 → α
20
P,Z SPECIFIED ?
NO
YES
21
0 → IPq,PZ
α2
ζ2
ζ1
ζ
23
P + 1 → W
24
W,q SPECIFIED ?
NO
YES
26
αn+1 → α
22
P, q → X
P,Z → Y
27
P,q → X
W,q → Y
ζ
ζ1
ζ2
25
0 → IPq,Wq
α3
θ1
θ2
θ
θ3
θ4
θ5
33
J + 1 → J
38
θ3 → θ
λ2 → λ
39
λ4 → λ
θ4 → θ
47
T > Tmax ?
YES
STOP
λ1
λ
λ7
λ6
β7
β6

1

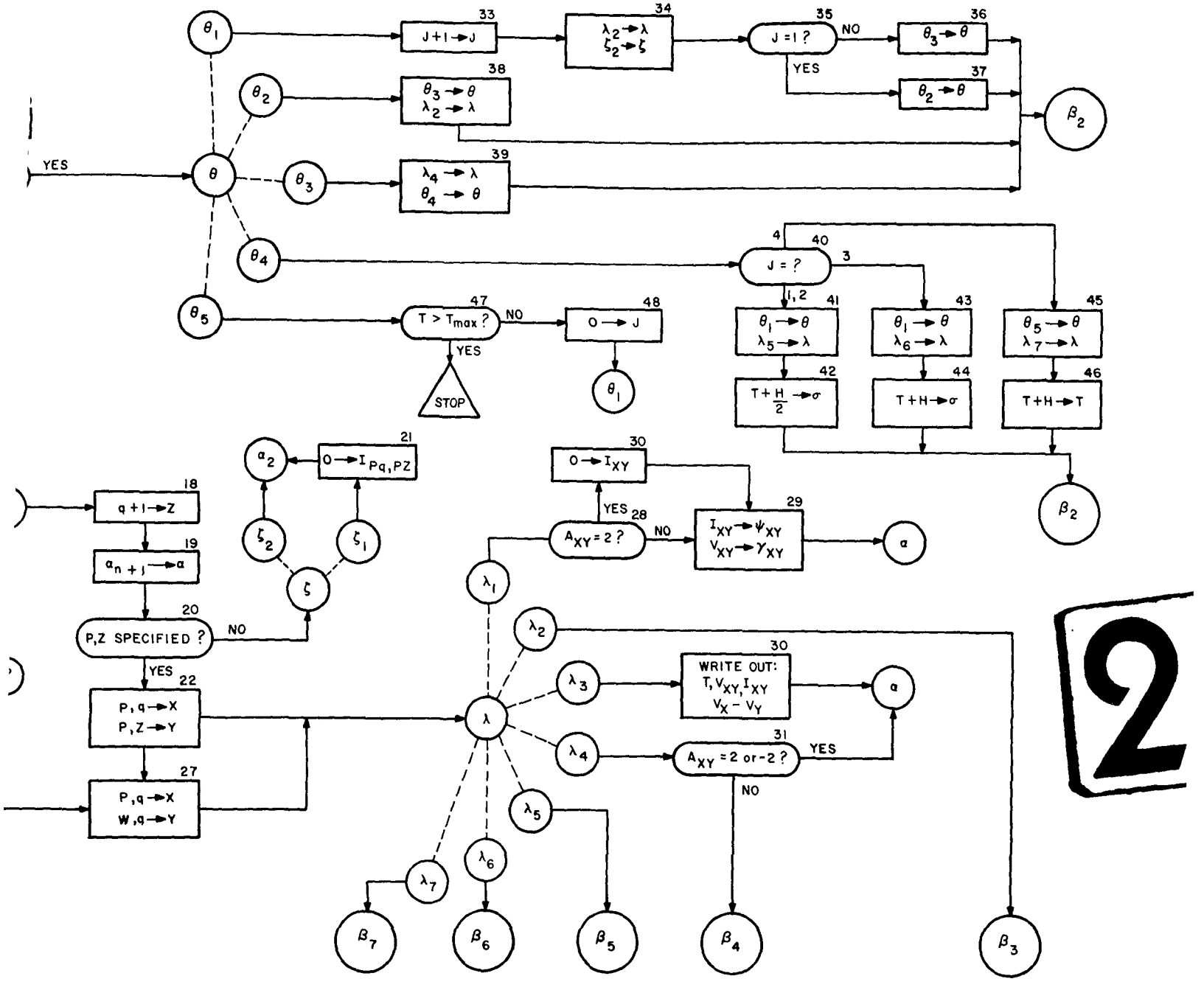
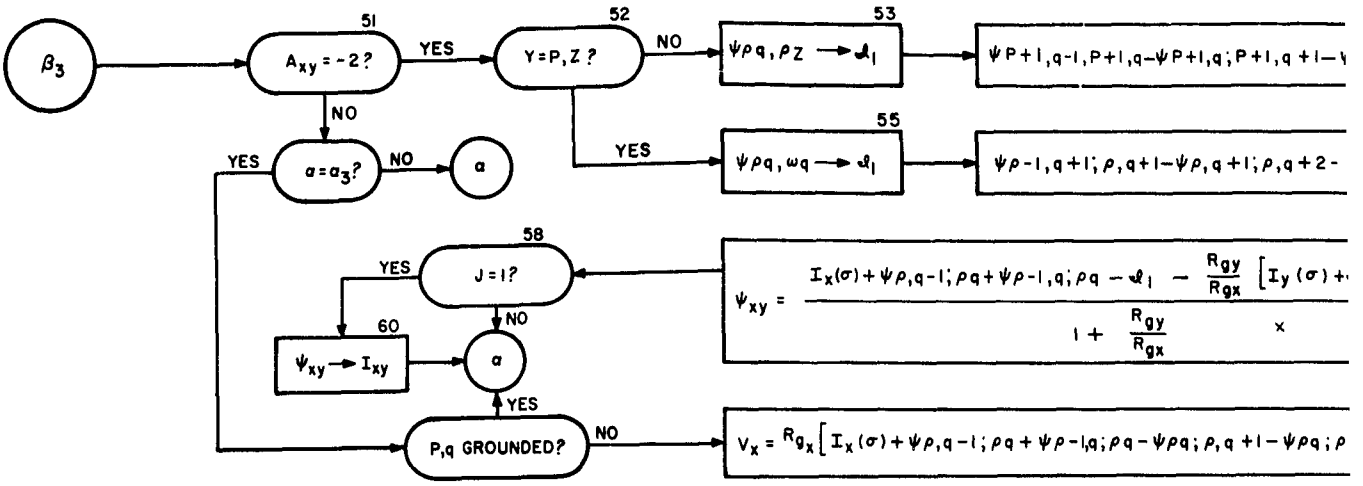
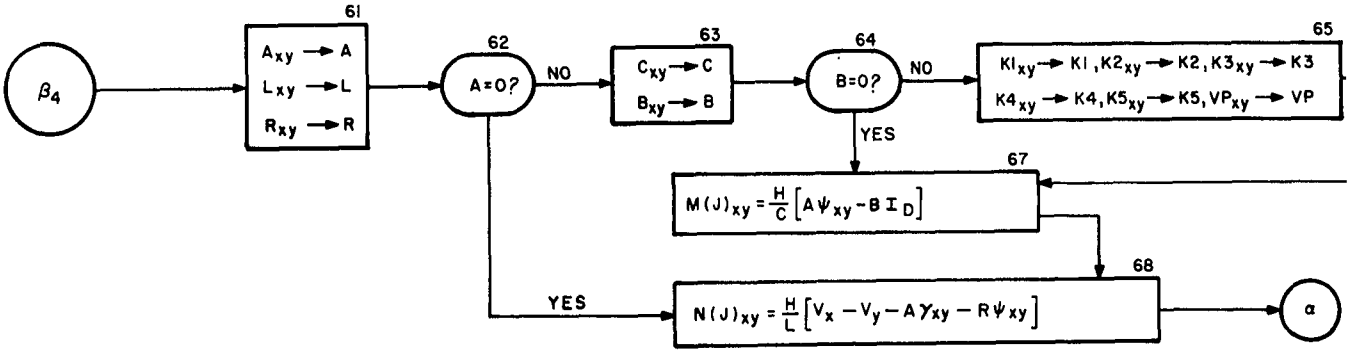
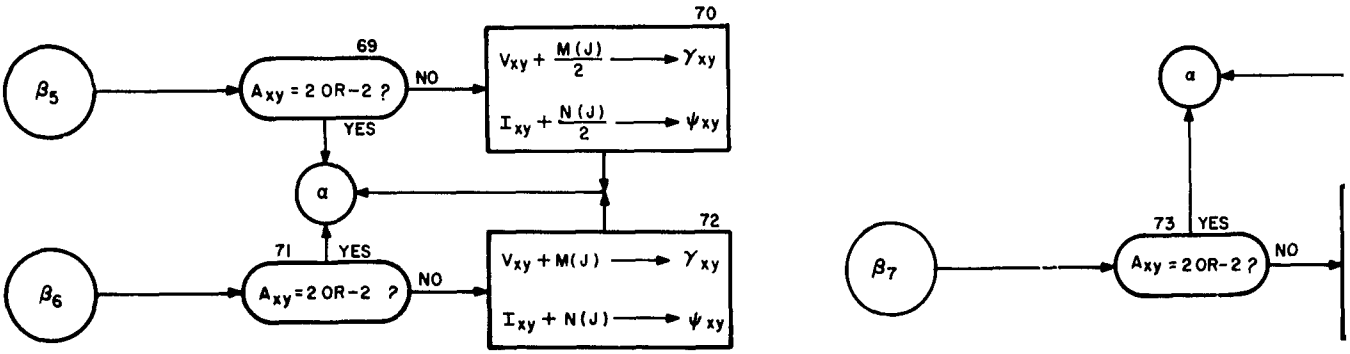


Figure I-4. *Flow Chart — General Program for Analysis of Linear or Non-Linear Circuit Problems using Fourth Order Runge-Kutta Method of Numerical Solution (sheet 2 of 3)*


β3
51
$A_{xy} = -2?$
YES
52
Y=P,Z ?
NO
53
$\psi\rho q, \rho Z \rightarrow \mathcal{L}_1$
$\psi P+1,q-1,P+1,q-\psi P+1,q;P+1,q+1-$
NO
$\alpha=\alpha_3?$
NO
α
YES
55
$\psi\rho q, \omega q \rightarrow \mathcal{L}_1$
$\psi\rho-1,q+1;\rho,q+1-\psi\rho,q+1;\rho,q+2-$
58
J=1?
YES
NO
60
$\psi_{xy} \rightarrow I_{xy}$
α
YES
P,q GROUNDED?
NO
$\psi_{xy} = \frac{I_x(\sigma)+\psi\rho,q-1;\rho q+\psi\rho-1,q;\rho q-\mathcal{L}_1 - \frac{R_{gy}}{R_{gx}}[I_y(\sigma)+}{1+\frac{R_{gy}}{R_{gx}} \times}$
$V_x = {}^{R}g_x[I_x(\sigma)+\psi\rho,q-1;\rho q+\psi\rho-1,q;\rho q-\psi\rho q;\rho,q+1-\psi\rho q;\rho$


β4
61
$A_{xy} \rightarrow A$
$L_{xy} \rightarrow L$
$R_{xy} \rightarrow R$
62
A=0?
NO
63
$C_{xy} \rightarrow C$
$B_{xy} \rightarrow B$
64
B=0?
NO
65
$K1_{xy} \rightarrow K1, K2_{xy} \rightarrow K2, K3_{xy} \rightarrow K3$
$K4_{xy} \rightarrow K4, K5_{xy} \rightarrow K5, VP_{xy} \rightarrow VP$
YES
67
$M(J)_{xy} = \frac{H}{C}[A\psi_{xy} - B I_D]$
68
YES
$N(J)_{xy} = \frac{H}{L}[V_x - V_y - A\gamma_{xy} - R\psi_{xy}]$
α


β5
69
$A_{xy} = 2$ OR -2 ?
NO
YES
70
$V_{xy} + \frac{M(J)}{2} \rightarrow \gamma_{xy}$
$I_{xy} + \frac{N(J)}{2} \rightarrow \psi_{xy}$
α
β6
71
$A_{xy} = 2$ OR -2 ?
YES
NO
72
$V_{xy} + M(J) \rightarrow \gamma_{xy}$
$I_{xy} + N(J) \rightarrow \psi_{xy}$
β7
73
$A_{xy} = 2$ OR -2 ?
YES
NO
α

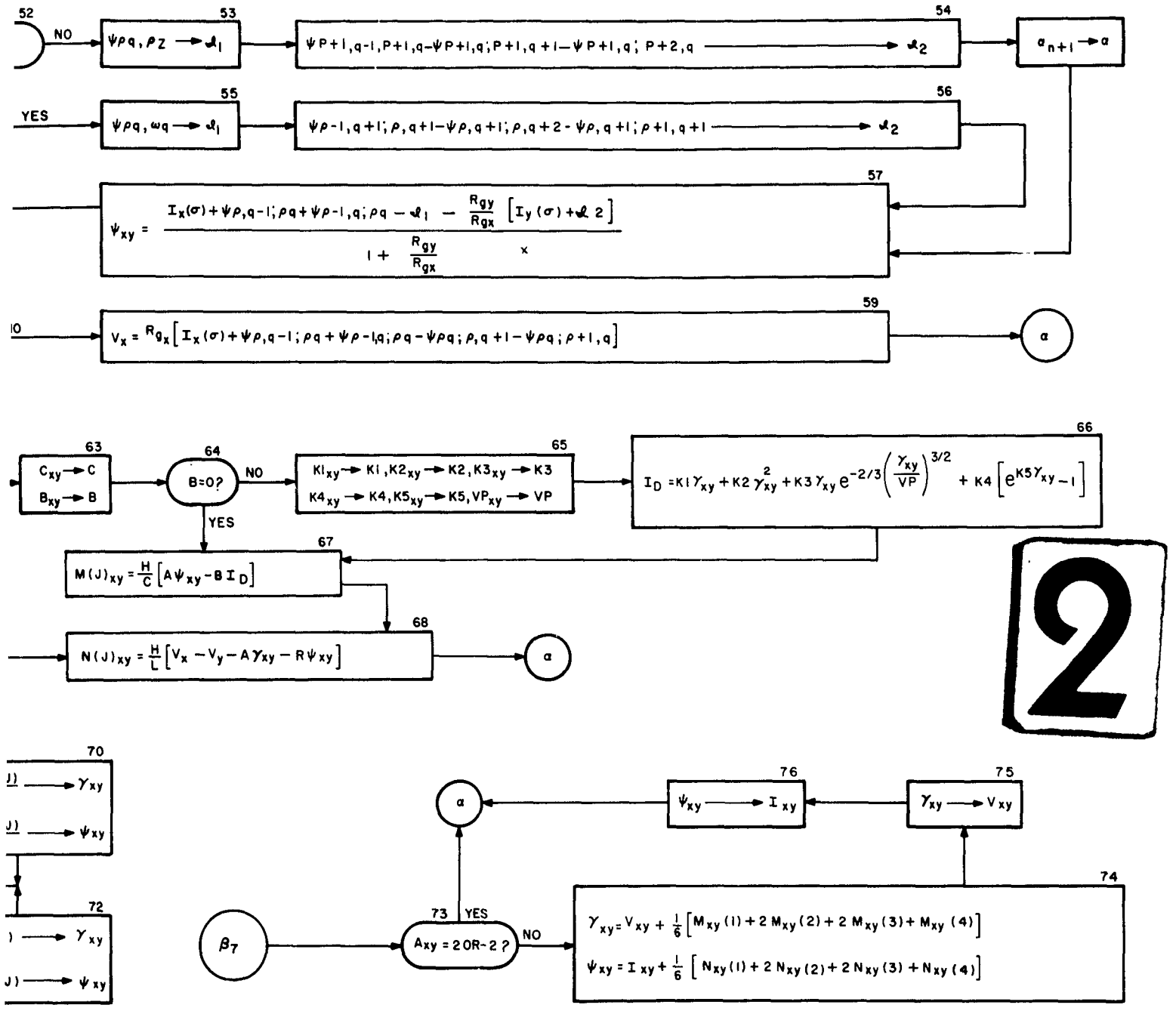


Figure I-4. Flow Chart — General Program for Analysis of Linear or Non-Linear Circuit Problems using Fourth Order Runge-Kutta Method of Numerical Solution (sheet 3 of 3)

Although the general ideas presented here are applicable to other methods of numerical solution, the flow chart accompanying this text was developed using the fourth order Runga-Kutta method[2]. The increment of time used in the solution depends not only on the accuracy desired, but also on the type of problem. In general, a time increment, H, should be at least less than one-quarter of the period of the smallest oscillation expected in the result.

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2. Introduction to Numerical Analysis by F. B. Hildebrand published by McGraw-Hill, 1956.